INVITED PAPER

Signal Integrity Flow for System-in-Package and Package-on-Package Devices

Signal degradation in these packages can be avoided by a practical design process that uses appropriate rules to simplify modeling, simulation, and analysis.

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ABSTRACT | As data rates required for systems in package (SiPs) increase and their complexity increases, signal integrity issues become increasingly difficult to address. The design flow of the SiP should therefore take into account these issues from the beginning. A design flow aimed at designing the SiP tracks is presented; its suitability for the design of packages comprising multiple stacked memories is verified through a design example. The proposed flow for signal integrity can be integrated easily within the complete design of the SiP.

KEYWORDS | Crosstalk; ground bounce; package on package (PoP); parasitics; system in package (SiP)

I. INTRODUCTION

New technologies generate new problems, as the saying goes. Systems-in-package (SiPs) [1]–[7] are no exception; in fact, the increasing number of applications this technology is required to address implies increasingly tougher requests for speed, heat dissipation, package dimensions, and cost. While the first generation of these "multiple devices" had just some heat removal issues, and no electrical problems, the present and future generations will be required to sustain high to extreme data rates: this implies the utmost attention to signal integrity aspects in the design of the various tracks linking the chips to each other and to the external world.

Signal integrity problems of an SiP package are inherently different from those of any other package but also differ from printed circuit boards (PCBs) or integrated circuit (IC) design. It is not just a matter of orders of magnitude. Differently from a standard package, the substrate of an SiP comprises various tracks at various connection levels, but cost as well as mechanical constraints do not allow using each other level as a ground plate, as high-performance PCBs do. The problem of mutual capacitances and inductances is therefore much more complex since it is not possible to consider each connection like a stripline with well-defined characteristic impedance.

The problem is instead fully three dimensional, as is the case of most IC connections. But of course physical dimensions are bigger than ICs, long bonding wires may be present, and relatively wide current loops may not be avoided, so that inductance issues are always present. Furthermore, the electrical model of the various interconnections may be not completely defined as is the case of an IC: the connections to the external world need some sort of modeling of the electrical behavior of the unknown "external world" of the package.

Of course, it is possible to inherit ideas and procedures from well-established signal integrity design flows addressed to the PCB and/or IC worlds, but they need be at least modified to be adapted to the new situation. Speaking of a signal integrity flow means also to include this specific flow into the entire system design. This includes mechanical and thermal aspects as well as the design of the single chips and of course testing methods. In Section II, two different package types are introduced; the problems for signal integrity they generate are highlighted. In Section III, we

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introduce some heuristic rules that can be used by the substrate designer to generate a first map of the electrical connections that is respectful of signal integrity issues. In Section IV, the signal integrity flow is discussed and a design example commented in its most important aspects.

II. SiP VERSUS PoP: PACKAGE EFFECTS ON SIGNAL INTEGRITY

The various chips assembled within a multichip package need be connected to each other and to the external world—i.e., to the package external leads, typically microballs. Two main technologies are in use at present. The first one, system in package, consists basically in including many chips in the same package, which serves not only as a mechanical support and a means for connecting the bonding pads on each chip to the external world but also as a first level of interchip interconnection. The bottom of the package, called substrate, is laminated with two or more metal interconnection levels that electrically couple the various chips to each other and to the external world. A particularly interesting SiP type actually stacks various chips thinned up to some tens of micrometers one on top of the other. Each chip is bonded to the substrate with wires whose length is fairly long if the chip is on top of the stack. The electrical parasitic of the long interconnections resulting from long bonding wires and long tracks in the substrate are likely to introduce undesired effects, which lead to signal integrity degradation [8]. They are *delay* due to slowed-up transitions of the signal (rise time, fall time) and transmission-line effects; *crosstalk* due to capacitive and inductive coupling between closely spaced tracks in the substrate; and *ground bounce* that causes undesired power supply and ground voltage oscillations. In particular, oscillations of the output-buffer-dedicated power supply (Vddq) can impact buffer commutation speed. These effects may be synergic in determining intersymbol interference (ISI), which consists in signal distortion high enough to cause previous symbols to affect the current one. If such effect is significant, determining the logical value of the present symbol may be difficult, if even possible. Package on package (PoP), whose cross-section is shown in Fig. 1, offers more flexibility than SiP in terms of manufacturability. Its structure consists of two separated ball grid array packages called PoP-top and PoP-bottom, assembled and tested separately but designed to be soldered together, so that the PoP-top contact balls match the land pads placed on the POP-bottom upper side. JEDEC package specifications ensure fully mechanical and electrical compatibility when they are soldered together and to the final PCB, assuring therefore perfect matching and preventing any coplanarity issue. PoP-top may include memories like flash NOR, flash NAND, and RAM chips, while PoP-bottom generally consists of an application-specific integrated circuit (ASIC) chip. The same JEDEC

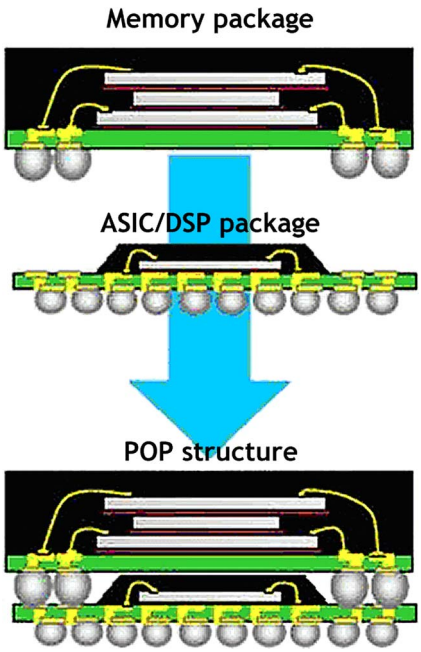

Fig. 1. *Illustrates the package on package concept.*

specifications define PoP mechanical dimensions: typical body size is 12×12 or 15×15 mm^2, which means that the substrate area is bigger than that of a typical memory SiP. Clearly this implies longer wire tracks in the routing of the substrate, which can impact I/Os' electrical performance. However, there may be a single advantage in this configuration, as signal integrity is concerned; that is, the "outside world" is normally connected only to the ASIC in PoP-bottom. Each signal connection of the PoP-top is with PoP-bottom, so their modeling has no uncertainty if the ASIC electrical characteristics are known, correct terminations can be established, and the resulting data links fully tested. However, PoP-top and PoP-bottom are likely fabricated by different vendors who do not disclose sufficiently detailed I/O characteristics of their chips to each other, so that residual uncertainty may still be present. At any rate, the tracks connecting the PoP-bottom I/O to the external world may be made short and therefore the design of such tracks becomes quite similar to that of a standard chip (Fig. 2). In the following, we shall consider the very common case of a memory SiP or PoP, made of a number of memory chips and perhaps a baseband die.

III. PRELAYOUT RULES

A. Prelayout Design Rules

As already discussed, interconnects at the package level can degrade the quality of digital signals [9]. Before designing the substrate, it is therefore necessary to obtain a

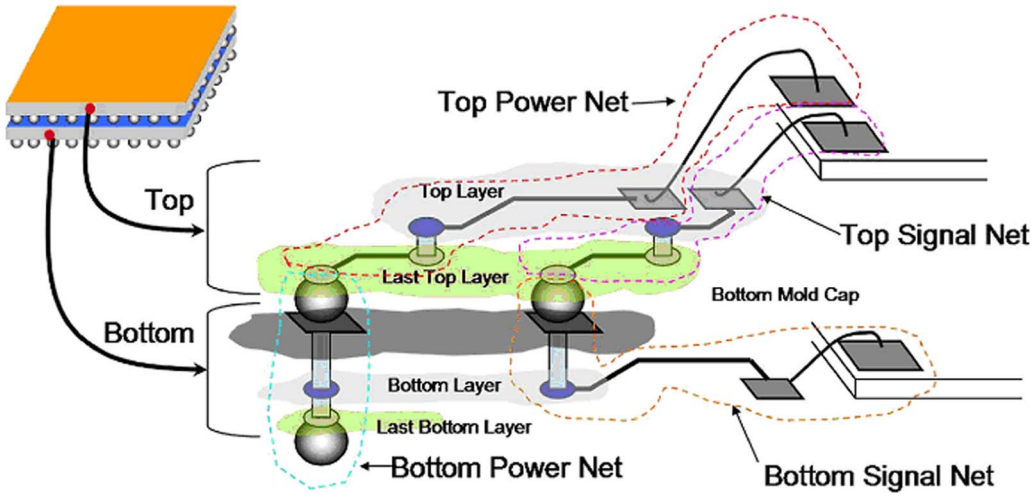

Fig. 2. ***Showing electrical connections between PoP-top and PoP-bottom for power supplies.***

preliminary set of information regarding such characteristics as output buffer strength, operative frequency, external load, and so on. These preliminary information impact the substrate layout in terms of routing, maximum length, and width of tracks. For example, reducing the memory speed from full to half or quarter will make reflections and ringing smaller, and this means having more design margin to design the substrate tracks. Once the operative frequency is established, some constraints are set, i.e., the maximum delay acceptable on the data bus, which in turn calls for an accurate routing of ground and power nets. Such time constraints have to be guaranteed even with highly capacitive loads at the package outputs (30 pF is usually reported in the datasheet). In high-speed designs, however, modeling the external load with a simple capacitance is not sufficiently accurate; however, the package designer usually does not know the whole characteristics of systems. Reasonable hypotheses are therefore formulated, and possibly referred to the final user, in order to evaluate the maximum impact of the package and so to determinate prelayout constrains. A typical simple model may consist of a transmission line and a load capacitance. In the particular case of a PoP, it may happen that the designer does not know the electrical characteristics of the bottom package (i.e., its maximum driven capacitive load and the characteristics of the power network) and also in this case some reasonable hypotheses have to be made. The following simple rules represent guidelines that a signal integrity engineer should take into account when designing a substrate; the rules are in order of importance for their effects on integrity of signals.

1) *Buffer supply nets* (ground and supply voltage [10], [11]). These tracks should be the first to be designed. They can impact the delay on the data bus due to Vgs modulation and the worsening of the signal transition time. The bouncing of supply voltage and ground levels generated at the ends of the transitions can impact the noise margin. In order to determine the maximum inductance associated to each buffer power supply subnet (that is, the track connecting the pad to the ball), the maximum of the current slope $(dI/dt|_{\max})$ has to be evaluated. Then

$$L_{al} \leq \frac{\Delta V_{\max}}{N \cdot \frac{dI}{dt}\Big|_{\max}} \tag{1}$$

where $\Delta V_{\max}$ is the maximum ground bouncing peak allowed in order to respect the constraints and N is the maximum number of buffers connected to each supply and ground pad that can change their logic state at the same time. In turn, $\Delta V_{\max}$ is obtained by considering the maximum delay increase caused by the reduction of the supply voltage and the maximum noise tolerated on the power supply voltage. The various subnets have to be connected together as close as possible to the output ball. In fact, when two subnets are interconnected, the track from such point of interconnection to the ball carries the current of both subnets. So, the ground bouncing associated to such common path is affected by the sum of the two current slopes, which increases therefore the noise. To guarantee the respect of the constraint obtained from (1), it is possible to create more parallel paths from a pad to the correspondent ball in order to reduce the parasitic inductance and to optimize the reference voltages. The buffer supply nets are the most critical also from the crosstalk point of view, since the current

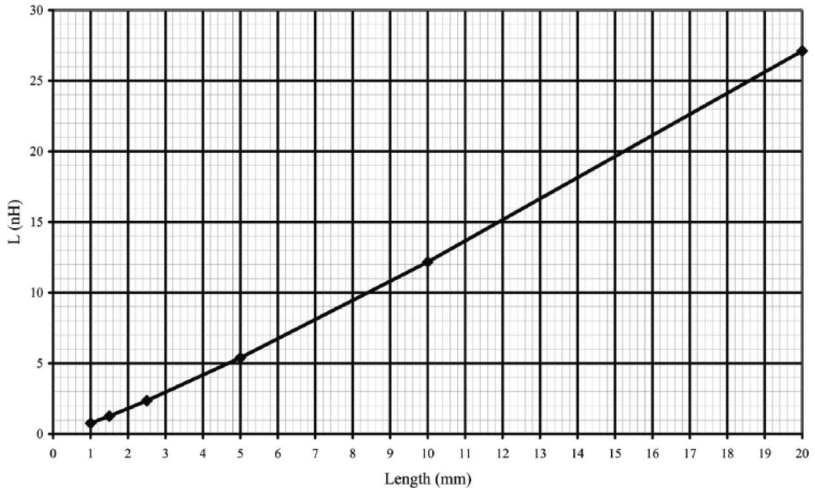

Fig. 3. ***Inductance of the substrate tracks (50 by 25 μm of section) in function of the length.***

that flows in them presents the maximum slope. It clearly appears that these tracks are one of the major concerns in substrate design and have to be routed with particular care.

2) *Core supply nets* (of the digital and analog circuitries). In order to estimate the requirements for the critical core supply tracks, a simple model consisting in the current generator Ib may be used. This current source is the main element of the integrated circuit electromagnetic model [12]: it sums the contribution of all the logic gates to the current circulating between the power supply pins of the memory. This means to simulate the chip current consumption. Based on such analysis, it is possible to establish some prelayout design rules to reduce the bouncing generated and to estimate the crosstalk between adjacent nets.

   Of course, the interconnections with the buffer supply nets should be avoided in order to prevent noise problems. The ground bouncing generated by the buffer signal transitions can impact the correct working of the critical circuitries (i.e., the reference voltages of the sense amplifiers). If such interconnections cannot be avoided, the connection point should be as close to the ball as possible.

3) *Data bus*. Such tracks are the main outputs (more precisely I/O) of a memory and thus their buffers have to drive the external loads. The length of the data tracks can affect the signal integrity because the inductance of the whole current loop can create over/undershoots. They are also critical for the possible presence of crosstalk between adjacent wires. Neglecting the mutual coupling between the power and ground nets and the signal track, the maximum inductance of the signal path can be evaluated as the difference between the inductance of the whole loop and that of the supply nets [8].

4) *Control signals*. The control signals can be critical because they can compromise the correct device behavior. A substrate designer has to pay attention to the crosstalk with other signals, monitoring the length of the subtrack adjacent to the critical nets in order to prevent unexpected operations. In particular, when the memory has two different pads and they must be connected to the same ball, the two nets should be designed with equal length, in order to avoid the skew between the signals.

5) *Other signals*. Based on practical experience, other signals (for example the addresses) are not so critical because they have more noise rejection rate. They can be immune to impulses superimposed to the signal and they can be affected only if the noise is present for sufficient time.

After having evaluated the maximum inductance of the critical nets, such electrical constraints can be transformed into geometrical characteristics of the tracks as shown in the following formula:

$$L = 2 \cdot 10^{-1} l \left[\ln\left(\frac{2\pi l}{W}\right) - 1 + \frac{W}{2\pi l} \right] \qquad (2)$$

where W and l are, respectively, the width and length of the tracks [13].

Figs. 3 and 4 show that in order to reduce the inductance of the critical nets, it is necessary to create as short as possible paths from pad to ball and to increase their width as much as possible. It is clear, however, that the inductance is more dependent on the track length than

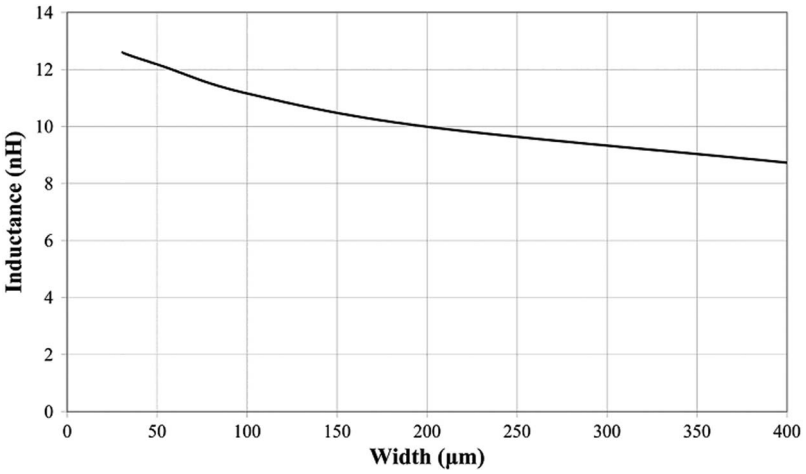

Fig. 4. *Inductance of the substrate tracks (25 μm of height by 1 cm of length) in function of the width. At the moment, 50 μm is the typical minimum for a substrate track.*

on its width. In the following, a few examples of recommendations are given.

- Regarding DQ (data nets), it is better to increase the room between DQ and to interdigitate them with power or ground tracks to reduce crosstalk effects. Make all the DQ with the same lengths to avoid skew on signals.
- Draw the tracks in metal 1 and in metal 2 in orthogonal directions, in order to reduce the crosstalk.
- Check the length of the subtracks adjacent to the critical nets in order to prevent unexpected operations. For example, the coupling between the chip enable signal and another track can create oscillations superimposed to the enable voltage, which can disable the chip.

B. Parasitic Extraction

Lumped models with fixed components values are useful in signal integrity analysis when the condition $\lambda \gg l$ is valid. This approximation breaks down when the working frequency increases [1]. More complex models are necessary in this case in order to include high-frequency effects like skin effects, radiation, and propagation delays. The use of "wide-band" models is essential to avoid errors in simulation results such as inaccurate delay, crosstalk, or simultaneous switching noise.

In circuit interconnections and package design, the structures are mainly three-dimensional (3-D) [14]. For many portions of this design, the significant interconnect may be long and uniform enough to be modeled using a two-dimensional approximation and transmission line theory (like on microstrip structures). Discontinuities in this design, such as vias through planes, chip-to-board connect, or width change on tracks, require full three-dimensional modeling.

Many methods and consequent numerical implementation have been developed in order to solve electromagnetic problems for this kind of structures [14], [15].

Approaches that have proven to be capable of detailed electromagnetic analysis of complicated integrated circuit interconnects are the accelerated integral equation methods like those used in FastCap [16] and FastHenry [17]. In this method, the Maxwell's equations are solved with magneto-quasi-static (MQS) assumption, in general 3-D structures may be simulated which a good accuracy from zero to some hundred MHz. Output of this solvers are RL matrix (that include also mutual inductive values between conductors) for FastHenry and the capacitance matrix for FastCap (that includes mutual capacitive values) [18]–[22].

Another common 3-D solver is Ansoft's Q3D Extractor.[1] This is a two-dimensional (2-D)/3-D MQS field simulator for parasitic extraction of electronic components and interconnections. Q3D Extractor utilizes the method of moments (MOM) and the finite element method (FEM) [22] to compute 2-D/3-D RLC parameters of a structure and automatically generates an equivalent SPICE subcircuit.

The frequency-dependent discretization of conductors, necessary because of skin effect at high frequencies, requires a very large number of filaments or surfaces, so these fast solvers are usable under MQS assumption only when computational costs are not prohibitive.

Several lumped models are obtainable once RLC matrix are known, like L-network [Fig. 5(a)], $\prod$-model [Fig. 5(b)], or T-model [Fig. 5(c)].

The different architectures approximate the real behavior of the substrate tracks with different bandwidth accuracy. In fact, the three lumped models are

[1]Ansoft, Pittsburgh, PA.

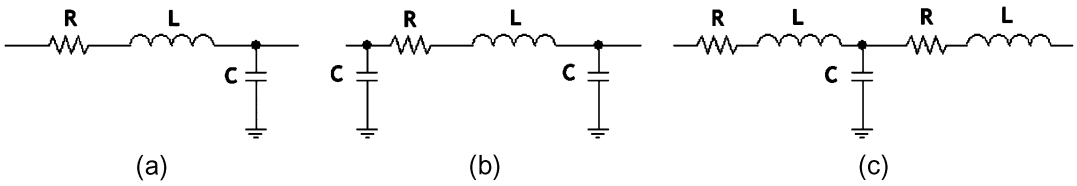

Fig. 5. *Different model for a single track.*

characterized by different transfer functions. Handbooks [1] suggest using the simple approximation shown in Fig. 5(a) if the signal bandwidth ($\omega|_{\mathrm{BW}}$) satisfies the following equation:

$$\omega|_{\mathrm{BW}} \leq \frac{0.1}{\sqrt{LC}}$$

and those shown in Fig. 5(b) or (c) if

$$\omega|_{\mathrm{BW}} \leq \frac{0.62}{\sqrt{LC}}.$$

Fig. 6 shows the general schematic used for two signal tracks and their return paths of ground (GND) and power supply (VDD). In the circuits, the coupling effects with other signal nets are modeled using coupled inductors and capacitors.

When the number of conductors becomes very large, also inductance and capacitance matrixes grow, and so does the computational cost. A reasonable solution is to set to zero the mutual inductance M coefficients lower than a given threshold (typically 5% of maximum value, without a significant loss of information on simulation). It is also possible to set to zero some values on the capacitance matrix (for example, it is sufficient to consider capacitance among adjacent conductor and not among distant conductors because of electrostatic shield effects). In a field solver, the user has to specify current sources and sinks, explaining if necessary whether they are multiple, in order to define the boundary conditions and to allow computing the electromagnetic field in the physical space of the system.

When MQS approximation is no longer valid, the full-wave analysis [23] should be preferred: it allows evaluating the electromagnetic wave propagation in both near and far fields. This latter approach is characterized by computing times so long as usually only a few sources (conductors) are considered.

IV. SIGNAL INTEGRITY FLOW

The signal integrity (SI) flow aims at optimizing the package impact and at verifying the performance (timing and signal logic levels) of the system, guaranteeing a satisfactory immunity to ground bouncing, over/undershoot, crosstalk, and ISI [24]–[27]. Here we will discuss the performance evaluation procedure of a device, applying it

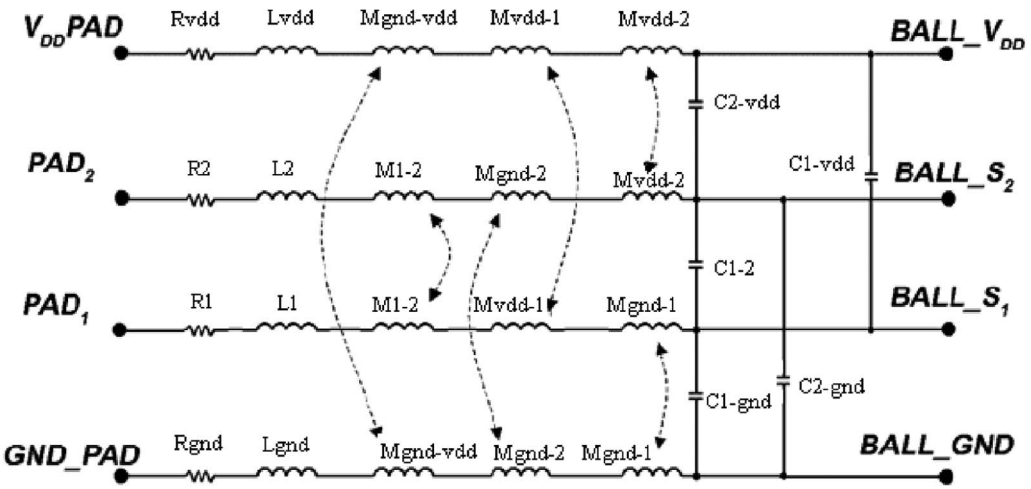

Fig. 6. *Schematic of interconnections of two signals (1 and 2) and two supply tracks (VDD and GND).*

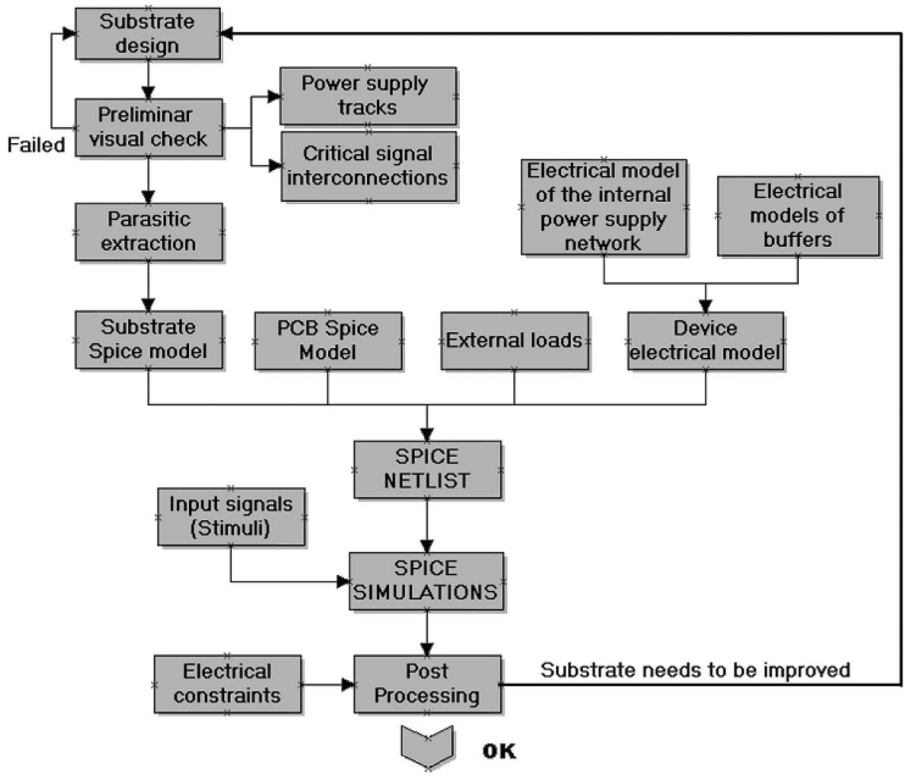

Fig. 7. ***Scheme of the signal integrity flow.***

to the project previously described. Fig. 7 describes schematically the SI flow, which is composed mainly of the following steps.

1) *Design of package substrate* based on prelayout empirical rules.
2) *Preliminary visual check* to estimate critical signals and to propose possible improvements of critical nets.
3) *Package parasitic extraction:* substrate is modelled by using lumped or distributed parameters [27], [28] or PEEC model [1]. In order to simplify the SI simulation, the coupling coefficients (mutual inductances and capacitances) below 5% of the maximum value are generally neglected.
4) *External PCB modelling*. Some hypotheses about the other devices of the system and about the external PCB are usually formulated in order to evaluate signal integrity and performance using a model close to the real application. The external PCB model strongly depends on the device typology (i.e., SiP or PoP). In effect, the PCB can impact on the power supply only or on the device signals as well.
5) *Receiver models*. The receiver characteristics might be unknown for SiP designers. Therefore, the package parasitic model and the capacitive pad loads of the receiver are estimated starting from a worst case analysis and from typical baseband characteristics.
6) *DUT models*. The I/O buffers of the analyzed device can be modelled by using a transistor level (TL) description. Although an SI simulation performed with TL model is very accurate, the computing time issue may suggest making use of other models (i.e., IBIS [29], [30], MPiLog [31]–[33], VHDL-AMS IBIS [34]–[36]). In addition, the power supply network internal to the die has to be modeled in order to evaluate ground bouncing phenomena and the correspondent delays on signals.
7) *Netlist*. The complete netlist, shown in Fig. 8, can now be obtained. Each part of the system that can affect signal integrity was in fact modelled and interconnections created.
8) *Input signals and simulations*. The Spice netlist is simulated by using suitable input waveforms. The best choice for the inputs is represented by a random pattern, which allows evaluating the noise generated under all working conditions. However, computing time can prevent a complete simulation. Therefore, preliminary simultaneous switching output (SSO; see Section IV-A) and pseudorandom bit sequence (PRBS; see Section IV-B) analyses are usually performed.

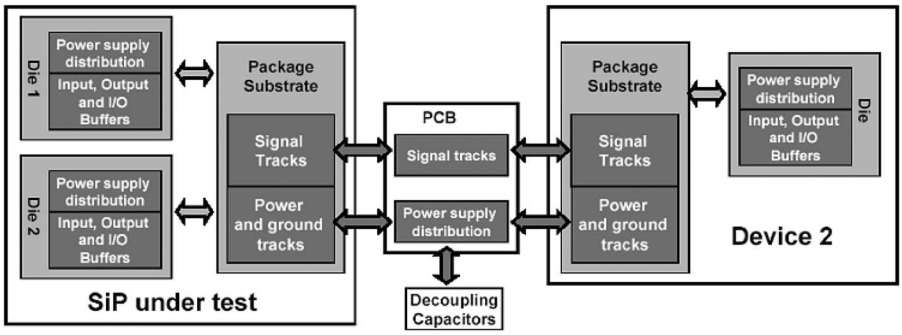

Fig. 8. ***Schematic used for the signal integrity analysis.***

9) *Postprocessing analysis*. The simulation results are analyzed in order to evaluate the presence of critical behavior and to guarantee the respect of the constraints.

A. SSO Analysis

SSO [37] is a kind of signal integrity analysis based on simulation results. The different signals involved in a single output signal transition are classified into functional groups. In the real operation of the device, such groups may switch simultaneously, which generates the maximum disturbance on the power and ground supply rails. Notice that in the simulation each signal switches once; therefore this analysis is not able to ascertain intersymbolic interference effects, and hence the maximum operative frequency of the device. On the contrary, SSO analyses aim at evaluating ground bouncing, delays, over/undershoots, and crosstalk introduced on active and quiet lines by a simultaneous switching of many signals.

It is necessary to define all the constraints imposed by the final application of the device in order to establish whether the above-mentioned effects compromise the performance of the system. The constraints can be graphically seen as "forbidden regions" in the voltage versus time plot of each signal, i.e., masks. Each mask depends on the kind of analyzed signal (power supplies, I/O signals, input signals, etc.) as well as on the performed analysis (crosstalks, rise or fall transitions, etc.). The different masks have to be based on the ideal signal, which is here defined as the signal simulated by neglecting the effects of the package. It is now possible to introduce the package effects and to evaluate whether the real signals stay within the mask limits. Fig. 9 depicts an example of a signal mask for the rise and fall transitions. In the example of Fig. 9, the maximum over/undershoot probed at the receiver input is equal to 0.4 V above and below the dc standard values in order to avoid any cross-conduction current events in the receiver and to prevent the electrostatic discharge (ESD) protection circuits from switching on. Actually, the threshold voltage of the ESD diodes is approximately equal to 0.5 V. The maximum tolerated delay (equal to 0.5 ns) is bound to the maximum

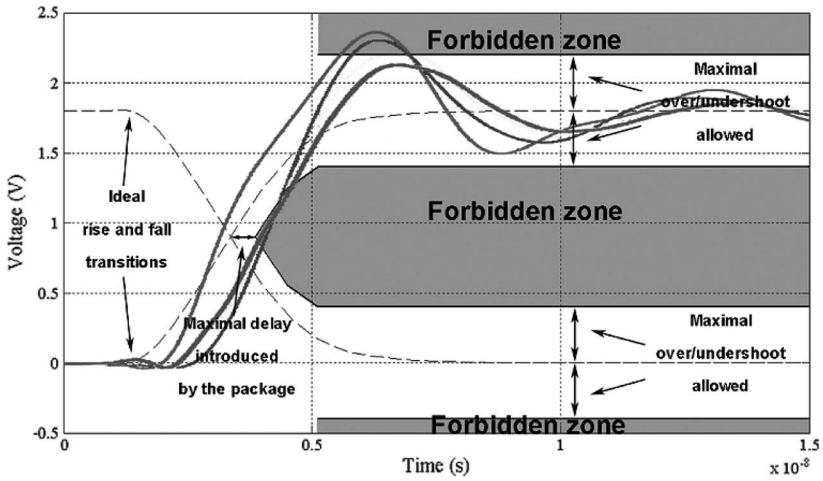

Fig. 9. ***Example of signals compared with the masks for rise and fall transitions.***

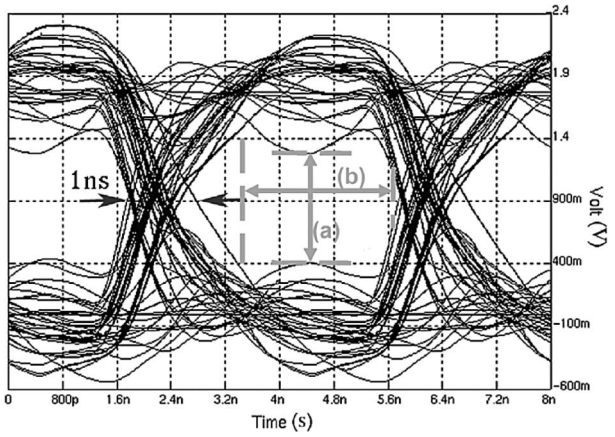

Fig. 10. ***Example of eye diagram of a critical system. (a) and (b) represent the vertical and horizontal apertures of the eye diagram, respectively.***

operative data transmission frequency for the device and to the performance illustrated in the datasheet.

B. PRBS Analysis

The PRBS simulation analysis aims at evaluating the behavior of the device at the typical and the maximum operative frequencies. It is performed by driving the input and output buffers of the various I/O lines by using pseudorandom patterns and is able to test signal integrity and to verify the correct working at the targeted frequency. Such an analysis allows estimating the ISI effect and the capability of the power supply network to dump the ground bouncing noise. The evaluation of the signal integrity is performed by plotting the eye diagram of the signals under test. Both vertical and horizontal apertures are controlled in order to comply with the voltage noise margin and, respectively, the time budget. In Figs. 10 and 11, two examples of eye diagram analysis [38] are shown. The first plot shows the eye diagram results for a design where package effects do not allow use of the device at the targeted frequency.

The second eye diagram shows an improved substrate design that allows operation at the targeted frequency. This was obtained by redesigning the power supply tracks to dump power and ground oscillations.

C. A Test Case

As a test case, we present the design of a PoP system comprising an ASIC in the bottom package and two stacked memories in the top package. The study is related only to the interface to the memories. A first step is a preliminary study to optimize the balls position in both packages, to guarantee the best performance for each device within the system. As usual, this solution is the result of an iterative process. There are various constrains that limit the solution space:

- package size;
- balls diameter and pitch;
- number of layers in the package substrate;
- dice geometry;
- technological and mechanical rules;
- thermal and electrical parameters.

Now we have to check the electrical impact of the produced interconnections network in both substrates. In Fig. 12, some critical tracks in the top and bottom package (power and data) are shown.

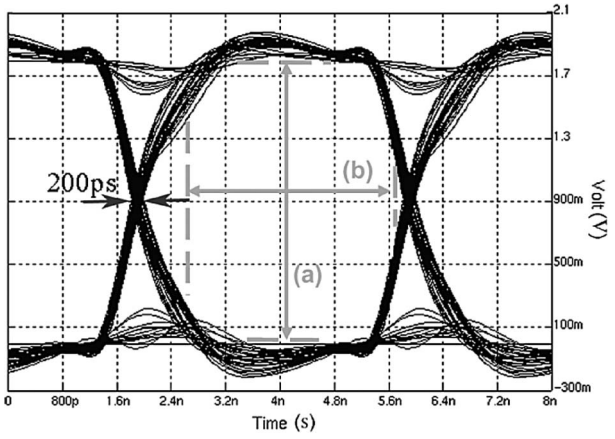

Fig. 11. ***Example of eye diagram for the device obtained improving the power supply network in comparison with that represented in Fig. 10. (a) and (b) represent the vertical and horizontal apertures of the eye diagram, respectively.***

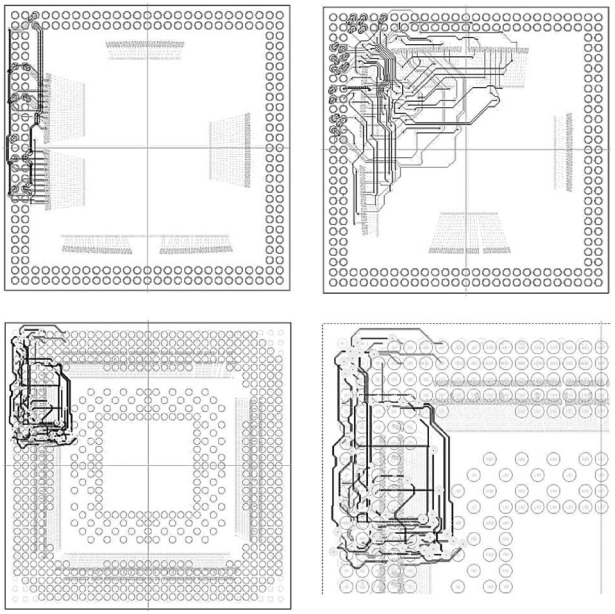

Fig. 12. ***PoP package substrates: power and data nets.***

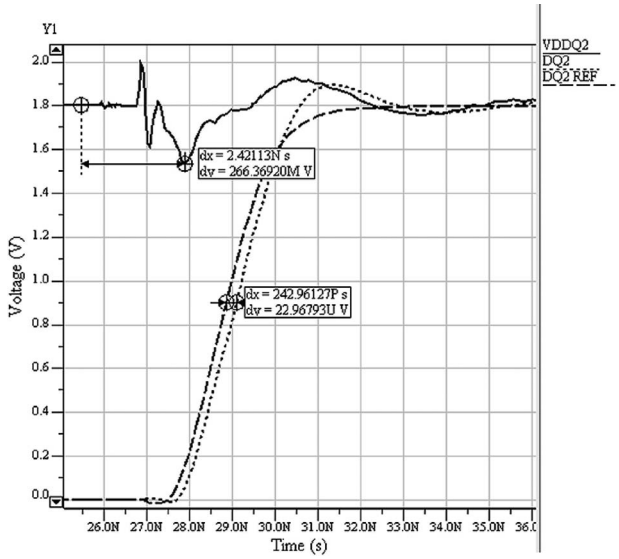

Fig. 13. ***PoP SSO analysis.***

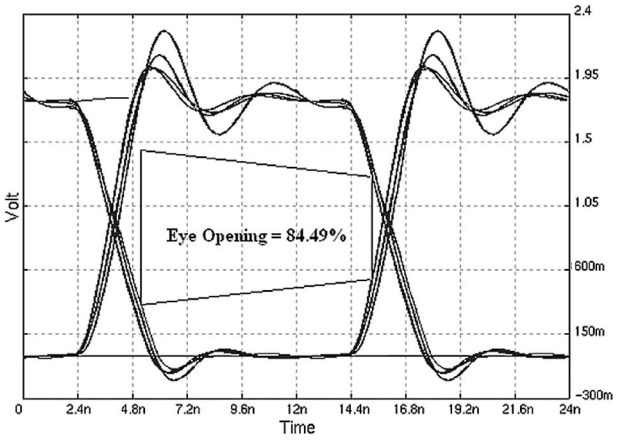

Fig. 14. ***PoP PRBS analysis.***

The electrical analysis can start when all the other checks are performed (manufacturability rules). As explained in [36], at this moment the only way to simulate the signals with realistic accuracy is by using transistor-level models for the buffers. In the following, we shall limit our analysis to two of the most important tracks in the device.

A first track to check is the power line; this is done by using the SSO approach. The memories I/O buffers are all driven at the same time in a low-to-high transition and vice versa to generate the maximum power consumption in order to test the correspondent power bouncing. In Fig. 13, the simulation results for an I/O signal on the die pad (with and without the top and bottom parasitic network to show the interconnection parasitic impact) and on the related power supply pad are shown.

It is relatively easy to verify if the minimum accepted peak value on the power rail is consistent with the maximum accepted delay on the data transition, which is determined by system considerations, in terms of time budget margin or/and buffer architecture and working frequency. In this test case, the target was a supply voltage negative peak lower than 300 mV and a correspondent delay lower than 300 ps.

After power integrity analysis, the other critical point to check is the data path, which is best done by using the PRBS analysis. Fig. 14 shows the eye diagram simulated for a victim track. The eye opening value is much better than the minimum required, which was derived from time budget considerations, and therefore the electrical constraints are satisfied.

V. CONCLUSION

We have shown that the signal integrity analysis in multichip packages is quite complex and has to be addressed from the beginning of the design. Guaranteeing the stability of the power lines is much more complex than in other designs due to the length of the related tracks, and therefore their inductance, that cannot be made unimportant in simple ways by using suitable capacitors. The nets in the substrate show high complexity; they are intrinsically three dimensional; and it is practically impossible to draw all of them as controlled impedance transmission lines. This calls for complex simulations and, sometimes, for ad hoc simplification of the resulting equivalent circuits. In this scenario, design methodologies based on some heuristics and successive time-consuming simulations to assess the correctness of the solution can be successfully employed. By using these methods, the authors were able to design an SiP from scratch within two weeks. ■

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