Prediction of Power Supply Noise From Switching Activity in an FPGA

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***Abstract*—Switching current drawn by an integrated circuit (IC) creates dynamic power supply noise on the IC and on the printed circuit board (PCB), which in turn causes jitter in *I/O* signals and reduces the maximum clock frequency. Predicting power supply noise is challenging due to the complexity of determining the dynamic current drawn by the IC and the impedance of the power delivery network. In this paper, a methodology is developed for predicting dynamic power supply noise on the PCB resulting from logic activity in a field-programmable gate array (FPGA). Time-domain switching currents within the FPGA are found by performing power simulations of the implemented logic over small time intervals. A high-frequency model of the die–package–PCB power delivery network is developed based on the inductance and capacitance of the package and die and a cavity model description of the PCB. The technique is shown to accurately predict noise on the PCB in both the time and frequency domains.**

***Index Terms*—Impedance, integrated circuit (IC), modeling, noise, power delivery network (PDN), power integrity.**

I. Introduction

POWER integrity is an increasing concern in modern digital designs. When millions of gates in an integrated circuit (IC) switch states after a clock edge, they draw substantial instantaneous current that causes noise on the power delivery network (PDN). This power supply noise can cause logical errors and can modify timing through logic circuits, which subsequently causes jitter and impacts data transmission rates and maximum clock speed [1]–[6]. The importance of power supply noise is growing as power supply voltages shrink and as data rates increase. Methods to accurately predict dynamic power supply noise would allow better determination of maximum jitter and maximum clock rates and would allow better assessment of noise mitigation techniques. Unfortunately, the complexity of modern ICs and the power supply delivery network makes this prediction difficult.

Determination of dynamic power supply noise requires an accurate description of the power bus impedance and of the current drawn by the IC. The power bus impedance includes the impedance of the die, the package, and the printed circuit board (PCB), including traces and power and return planes [1], [3], [6], [7]–[10]. The PDN of the die and package is typically described using a lumped-element model below a few gigahertz [11]. While a lumped-element model is sufficient for the die and package to gigahertz frequencies, a lumped-element model of the PCB power and return planes can break down at hundreds of megahertz, when the size of the PCB becomes electrically large [12]. One method of improving the model of the power and return planes of the PCB above a few hundred megahertz is to model their impedance as a summation of cavity resonant modes [12]–[15]. This technique allows the impedance of the PDN to be estimated both quickly and accurately. Together, the cavity model of the PCB and the lumped-element model of the IC form an accurate representation of the overall power deliver network [9], [10].

Power supply noise is generated by high-frequency currents drawn by the ICs. Most traditional computer-aided design tools only predict the average, or dc, current drawn by the IC in the process of predicting static IR voltage drops or average power usage, which is insufficient for predicting the noise. Dynamic current draw is typically obtained through SPICE or SPICE-like simulations [11], [19]–[21]. In these cases, logic components are simulated at the transistor level to generate a current waveform. Current waveforms may be found for simple components, like a logic gate, and then these waveforms may be added together to estimate the waveform for a larger component, like a processing block. In some cases, simulations are performed directly on the larger processing block, though in many cases SPICE simulations of large blocks is unreasonable with current simulation and processing tools. When predicting power supply noise, logic components are replaced by current sources representing the component's dynamic current draw. While studies have shown this approach to work well, in many scenarios, the engineer does not have access to the complete on-die design information required to estimate the dynamic current in this manner. Furthermore, for most practical designs, the simulation

Manuscript received December 10, 2012; revised August 1, 2013; accepted November 12, 2013. Date of publication January 1, 2014; date of current version May 19, 2014. This work was supported by the National Science Foundation under Grant no. 0855878.

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Digital Object Identifier 10.1109/TEMC.2013.2293872

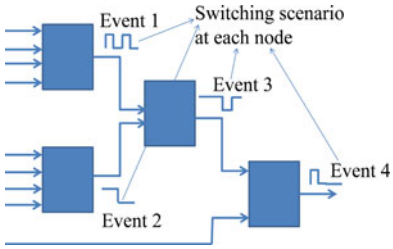

Fig. 1. Switching events propagate through a digital logic circuit from the inputs to the output.

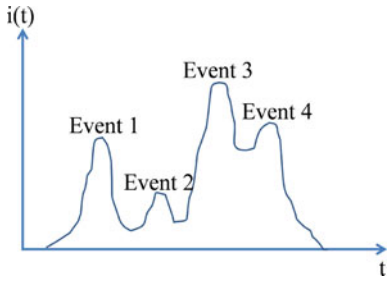

Fig. 2. Dynamic current is associated with the switching times and power draw of each gate.

times required to estimate the current can be unreasonably long without special purpose software for estimating current [11]. While dynamic current can also be found through on-die measurements [16], [17], measuring current is impractical in most designs.

The following paper presents an efficient methodology for predicting the dynamic current drawn by a design implemented in a field-programmable gate array (FPGA) and for predicting the resulting power supply noise. The transient current is estimated through simulation of the static power consumed by the FPGA over small intervals of time. The PDN of the FPGA die and package is modeled using an equivalent lumped-*RLC* circuit. The PCB is modeled using a cavity model. Together, the dynamic current along with the impedance model of the die, package, and PCB are used to predict the noise voltage observed at different locations on the PCB. Comparison of simulations and measurements shows that this technique can be used to accurately estimate the power supply noise in both the time and frequency domains.

II. Current Source Modeling

The ability to estimate dynamic current is not a part of most FPGA computer-aided design tools. Many tools, however, are built to find power. Dynamic current can be estimated from dynamic power by assuming that the power supply voltage is constant. While most software tools are only configured to estimate static power consumption, dynamic power can be estimated from the static power determined over small time intervals. The process is described next.

A typical digital circuit is shown in Fig. 1. Switching of inputs to the logical circuit generates a cascade of switching events as logical changes propagate from the input to the output. Switching at each gate draws current as illustrated in Fig. 2. Most current is drawn immediately after a clock edge, when the

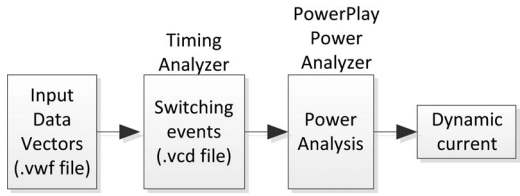

Fig. 3. Simulation of dynamic current.

inputs to the circuit change. Some current is drawn long after the clock edge, however, as logic circuits deep within the design switch after a long propagation delay of logical data through the circuit.

Given an input data vector, the logical function of each gate, and the propagation delay through each gate, it is relatively straightforward to estimate a timing diagram for logical switching at each gate output. If one knows the time of each switching event and the energy consumed by each event, one can then estimate the dynamic power or current for the circuit.

Dynamic current is estimated here using the PowerPlay Power Analyzer (PPPA) tool that is part of Altera Quartus II software suite [18]. This tool determines the power consumed by an FPGA for a particular logic circuit, given the clock frequency and time interval of operation. A logical simulation of the digital circuit is performed first using the Quartus II Timing Analyzer with a given data pattern applied to the circuit input as shown in Fig. 3. The timing analyzer generates a .VCD (value change dump) file which includes information about when and where switching occurs within the logic design. Power analysis is then performed using this .VCD file. While PPPA only estimates the average power draw, one option available in the tool is to perform a power estimate over a given period of time, determined by the start time, stop time, and/or time interval. By setting a small time interval, the average power over the interval becomes approximately "instantaneous" and can be used to estimate the "instantaneous" current. By repetitively performing this simulation over consecutive intervals of time, a waveform for the dynamic current can be obtained. This repetitive simulation can be automated using scripts and can be done relatively quickly.

In our work, an appropriate size for the time interval was determined experimentally. The noise waveform on the PCB was estimated for small and large time intervals. A small time interval results in a large number of points used to represent the current waveform, giving a high-resolution representation of the waveform but also increasing the computation requirements. An interval size was chosen that gave a good tradeoff between the quality of the estimated noise waveform and the computational requirements. In our simulations, intervals less than 1 ns did not improve estimates of noise voltages.

A simulation of the dynamic current was performed for a simple circuit consisting of many parallel T-flip-flops, as shown in Fig. 4. Each block in Fig. 4 represents many T-flip-flops in parallel. Tests were performed on an Altera Stratix II FPGA. Each block contains a sufficient number of T-flip-flops to consume 5% of the logical resources available in the FPGA. When the clock input transitions from low to high, the T-flip-flops in this block all switch state. The four blocks of T-flip-flops are driven by four different clock frequencies, so that they switch at different times. A clock divider generates a clock at 1/7, 1/3, 3/7, and

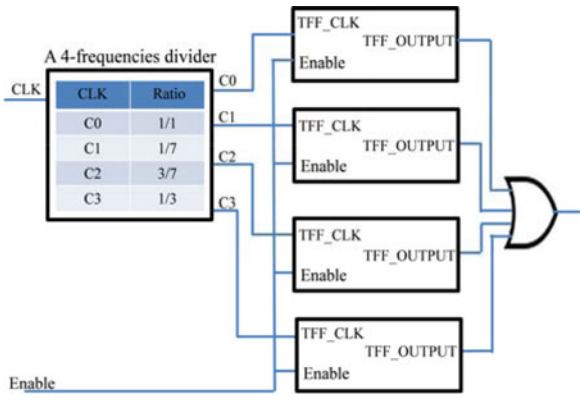

Fig. 4. Design utilizing T-flip-flops to generate switching at four different frequencies.

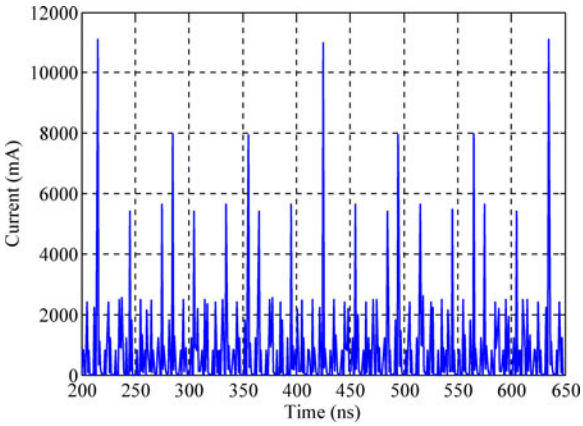

Fig. 5. Switching current drawn by the circuit in Fig. 4.

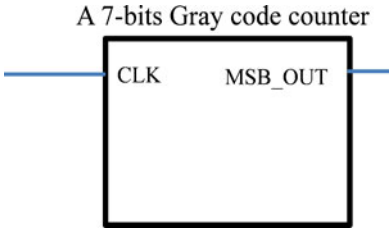

Fig. 6. 7-bit gray code counter.

1/1 of the clock frequency. Together, the four blocks consume 20% of the FPGA logical resources. Fig. 5 shows the dynamic current predicted using the methodology described previously. The waveform shows both the current consumed by the T-flip-flops as well as by the clock tree. Different sized peaks occur depending on the number of flip-flops that switch at a particular time. At the highest peaks, around 11 000 mA, all four blocks switch simultaneously. At the peaks around 8000 mA, the 1/7, 3/7, and 1/1 clocks switch together, and so forth. To test a more sophisticated circuit, tests were also performed using a 7-bit gray code counter, as shown in Fig. 6. Using a 100 MHz clock, the most significant bit of the counter changes with an oscillation frequency of 100 MHz/2^7 = 0.78 MHz. Many gray code counters were placed together in a large block, similar to the T-flip-flops in Fig. 4, so they would draw sizeable current and generate sizeable noise when they switched. All together,

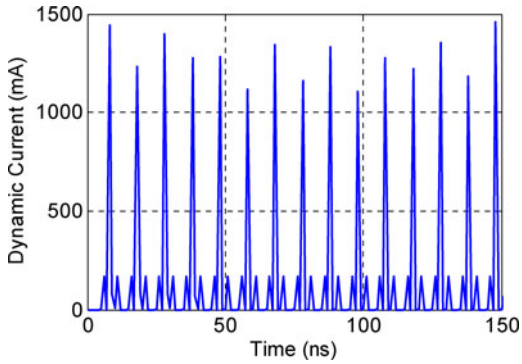

Fig. 7. Switching current drawn by the gray code counter.

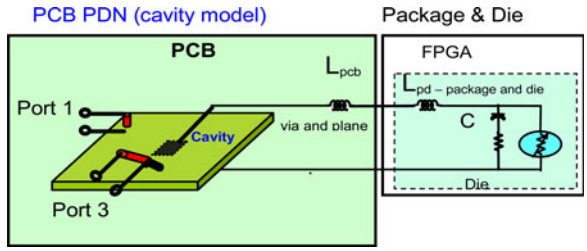

Fig. 8. Model of the PCB, package, and die.

the gray code counters consumed 5% of the FPGA logical resources. The dynamic current drawn by this 7-bit gray code counter block is shown in Fig. 7 for a 150 ns interval.

III. Impedance Modeling

The noise voltage on the PDN results from the switching current drawn by the FPGA and the PDN impedance. Estimation of the PDN impedance is explained later, first for a case where no decoupling capacitors are placed on the PCB and then for a case with decoupling capacitors.

A. Modeling the Die–Package–PCB

The PDN for the FPGA includes the on-die power delivery system, the FPGA package, and the PDN on the PCB. The PCB includes power and return planes, decoupling capacitors, and a low-frequency dc power supply. For estimating power supply noise on the PCB, the FPGA may reasonably be represented as drawing current from a single point on the PCB and, thus, the IC PDN can be approximated using a single lumped capacitor, inductor, and resistor, C_{FPGA}, L_{FPGA}, and R_{FPGA}, as shown in Fig. 8. L_{FPGA} represents the equivalent inductance of all the power and return pins of the package (package traces and balls). C_{FPGA} and R_{FPGA} represent the on-die capacitance and resistance. The switching current is placed in parallel with the on-die capacitance and resistance. For the FPGA used here, C_{FPGA}, R_{FPGA}, and L_{FPGA} were determined experimentally to be 440 nF (when powered), 10 pH, and 0.7 Ω, respectively, by comparing the measured impedance looking into the power and return planes of a PCB with and without the FPGA present. The on-die decoupling capacitance and package inductance act as a low-pass filter for the noise currents. Above the *LC* resonant frequency (76 MHz), this filter will reduce noise current through

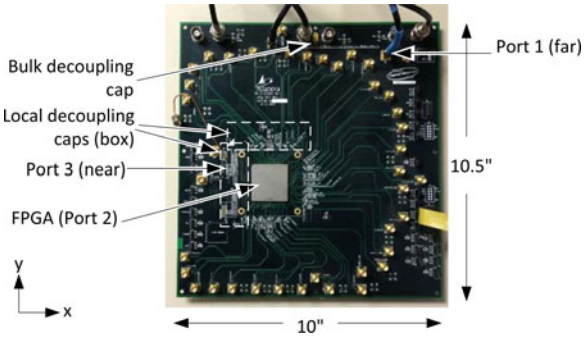

Fig. 9. Location of decoupling capacitors on the PCB.

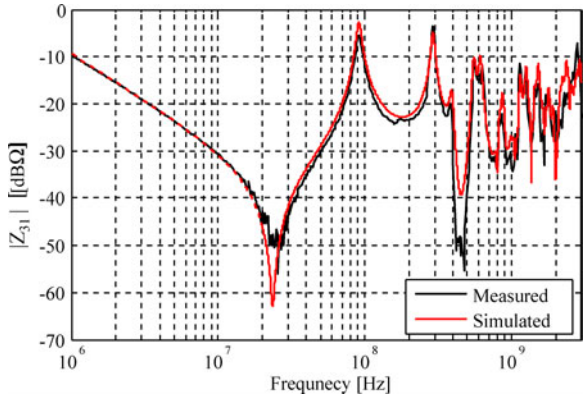

Fig. 10. Simulated and measured transfer impedance between ports 1 and 3 on the PCB.

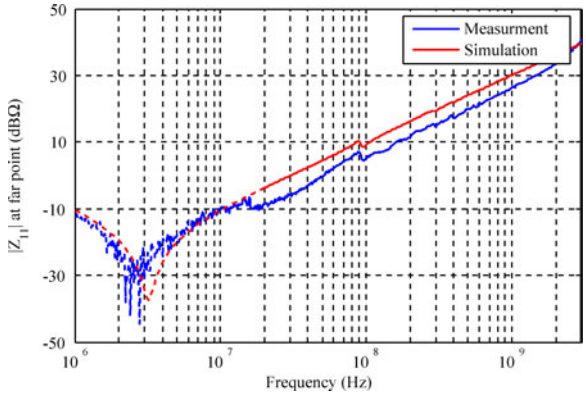

Fig. 11. Simulated and measured impedance looking into port 1.

the package by 40 dB/decade, so their values have a substantial impact on the high-frequency noise seen on the power and return planes.

The impedance of the power and return planes of the PCB were found using a cavity model [12]–[15]. The resulting impedance can be represented using either S-parameter blocks or using an equivalent SPICE network. To validate both the impedance response of the system and the resulting noise voltage, two measurement ports were placed on the PCB as shown in Figs. 8 and 9. The FPGA has three power supplies: a 1.3 V supply for the core, a 2.5 V supply for the I/O, and a 3.3 V predriver supply. The ports were placed between the 1.3 V supply plane for the core and the PCB return plane. Port 1 is relatively far away from the FPGA. Port 3 is relatively close. Port 2 is the location where the FPGA is connected to the PCB. On an X–Y grid with (0, 0) at the bottom left corner of the board, port 1 is located at (7.91, 9.25) inches, port 2 (the FPGA) at (3.5, 4.3) inches, and port 3 at (1.95, 4.63) inches. The cavity model of the PCB accurately represents the differing impedances seen among ports 1, 2, and 3. The input impedance of any measurement equipment attached to ports 1 and 3 is included in simulations. The model of the ports included a 6 nH parasitic inductance in series with the port, to model the connection to the power and return planes.

The low-frequency dc power supply was not modeled as a part of this effort. Measurements with and without the power supply connected to the PCB showed that the power supply had negligible impact on of the power-plane impedance within the frequency range considered in this study.

To help validate the power bus model, Z-parameter measurements were made between ports and the results were compared to the simulated values. Fig. 10 shows the measured and simulated values of Z_{31} when the IC was placed on the PCB. Measured and simulated values were within a few decibels at all frequencies except around 23 and 450 MHz, where the response at system resonances was under or overestimated by about 10 dB. The system resonances around 23 and 90 MHz are due to the lumped-element behavior of the die–package–PCB. The numerous peaks above 300 MHz are due to resonant modes within the cavity formed by the power/ground plane pair.

Fig. 11 shows the self-impedance, Z_{11}, looking into port 1. The measured and simulated values also agree here within a few decibels. The resonance around 3 MHz is due to the inductance of the connector at port 1 (6 nH) and the overall capacitance of the PCB and FPGA (roughly 440 nF). The small error in the simulated and measured values of impedance is due to a small error in the simulated value of the port inductance and the difficulty of making a good measurement of input impedance with a network analyzer when the impedance is much smaller than 1 Ω.

B. Modeling System Impedance With Decoupling Capacitors

Measurements and simulations were performed both with and without decoupling capacitors placed on the board. Decoupling capacitors were modeled as a lumped capacitor in series with an inductance associated with the equivalent self-inductance of the capacitor in series with the connection inductance to the power and return planes. The capacitors were added to the overall power bus model by placing ports at the capacitor location on the PCB power and return planes.

Measurements were performed with 16 decoupling capacitors (15 SMT capacitors and 1 330 uF bulk decoupling capacitor) placed on the PCB as shown in Fig. 9. The SMT capacitors were located near to the FPGA. The bulk decoupling capacitor was located near to the dc power supply. The bulk decoupling capacitor was modeled in series with a 15 nH connection inductance and a 60 mΩ resistance. The SMT capacitors included five 0805 10 μF capacitors, each modeled in series with a 1.2 nH connection inductance, five 0603 2.2 μF capacitors in series with a 1 nH inductance, and five 0603 1 μF capacitors in series with a 1 nH inductance.

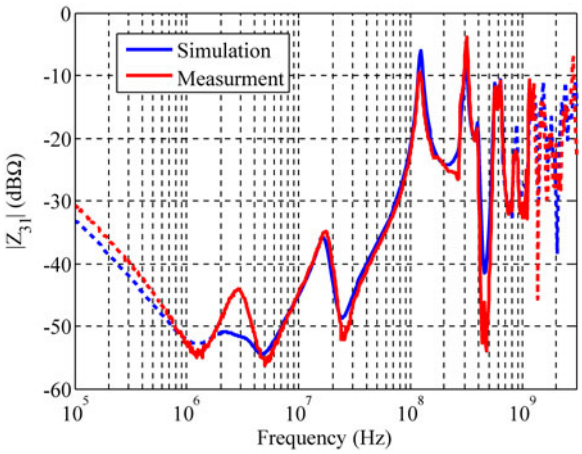

Fig. 12. Simulated and measured transfer impedance between ports 1 and 3 when 16 decoupling capacitors were placed on the PCB.

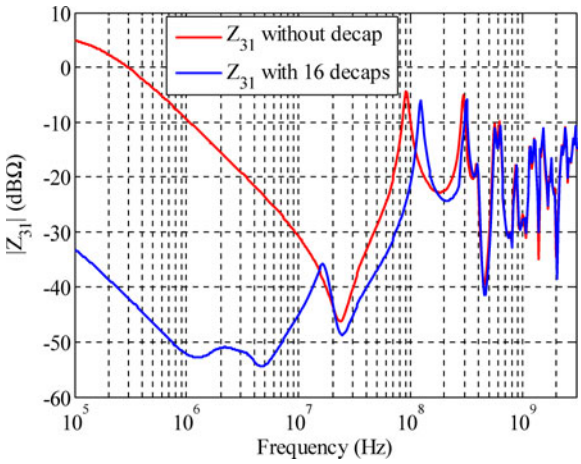

Fig. 13. Simulated transfer impedance between ports 1 and 3 with and without decoupling capacitors placed on the PCB.

The simulated and measured values of transfer impedance between ports 1 and 3, Z_{31}, are shown in Fig. 12 when the 16 decoupling capacitors were placed on the board. The simulated and measured impedance matches within a few decibels at all but a few frequencies. The small deviation between the measured and simulated impedances at low frequencies (less than 10 MHz) is due to a variation in the actual values of the capacitors about their nominal values, as specified in their datasheet and used in SPICE simulations.

The impact of adding decoupling capacitors to the PCB is illustrated in Fig. 13, where the transfer impedance between ports 1 and 3 is shown with and without the added decoupling capacitors. While the decoupling capacitors have a significant impact on impedance at low frequencies (i.e., below 100 MHz), they have very little impact at higher frequencies, due to the parasitic inductance to the capacitors.

IV. Noise Voltage

To evaluate the accuracy of the model, the switching noise voltage generated between the power and return planes was measured at port 1, far away from the IC, as indicated in Fig. 9. Measurements were made while the FPGA was loaded and running either the T-flip-flop or gray code design described in Section II. The noise voltage was measured using either an oscilloscope, for a time-domain measurement, or a spectrum analyzer, for a frequency-domain measurement. A signal generator was also connected to the FPGA to provide a 100 MHz clock signal. Measurements were performed in a shielded chamber to exclude interference from other sources. Measurements were made both with and without decoupling capacitors on the board.

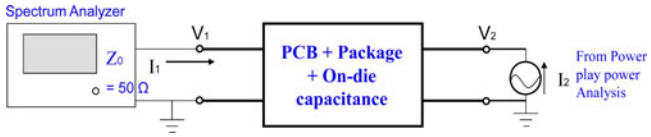

Fig. 14. Switching currents generate noise voltage at the oscilloscope through the impedance of the PCB, package, and die.

An equivalent circuit representing the coupling between the switching current in the FPGA and the noise voltage at the oscilloscope is shown in Fig. 14. The current source and oscilloscope are essentially connected to two ports of an impedance network. The relationship between voltage and current at each port is given in the frequency domain by

$$\begin{bmatrix} V_1(\omega) \\ V_2(\omega) \end{bmatrix} = \begin{bmatrix} Z_{11}(\omega) & Z_{12}(\omega) \\ Z_{21}(\omega) & Z_{22}(\omega) \end{bmatrix} \begin{bmatrix} I_1(\omega) \\ I_2(\omega) \end{bmatrix} \tag{1}$$

where $V_1(\omega)$ is the voltage at the spectrum analyzer or oscilloscope, $V_2(\omega)$ is the voltage inside the die, $I_1(\omega)$ is the current from the spectrum analyzer or oscilloscope, and $I_2(\omega)$ is the switching current in the FPGA as estimated from PPPA as described in Section II. Since the spectrum analyzer or oscilloscope acts as a 50-Ω load on the PDN,

$$V_1(\omega) = -I_1(\omega) \times 50\ \Omega. \tag{2}$$

Solving (1) and (2) gives the measured noise voltage in terms of the on-die switching current

$$V_1(\omega) = Z_{21}(\omega) I_2(\omega) \Big/ (1 + Z_{11}(\omega)/50) \tag{3}$$

where $Z_{11}(\omega)$ and $Z_{21}(\omega)$ are the input impedance looking into port 1 and the transfer impedance between port 1 and port 2, where port 2 is inside the die at the location of the switching current. While estimates using (3) can be directly compared to spectrum analyzer measurements, the inverse Fourier transform of (3) can be used to estimate the time-domain noise voltage and can be compared to oscilloscope measurements.

A comparison of the measured and simulated noise voltages at port 1 is seen in Figs. 15 and 16 when the T-flip-flop pattern was implemented inside the FPGA. Fig. 15 shows the spectrum, as measured with the spectrum analyzer, and Fig. 16 shows the time-domain noise waveform, as measured with the oscilloscope. These results were generated without decoupling capacitors on the board. A dc component is not observed in these results, as the measurements were made using a dc block and as only the (ac) switching sources were modeled in simulation, not the dc power supply. The measured and simulated spectra generally match within a few decibels with the exception of a few low-frequency (and low-amplitude) components at roughly

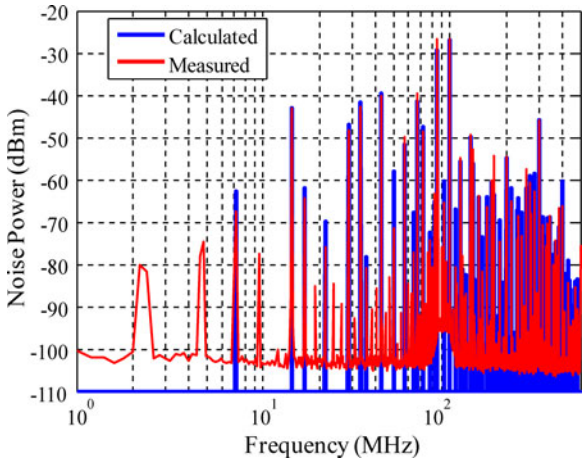

Fig. 15. Noise voltage spectrum at port 1 when implementing the T-flip-flop design.

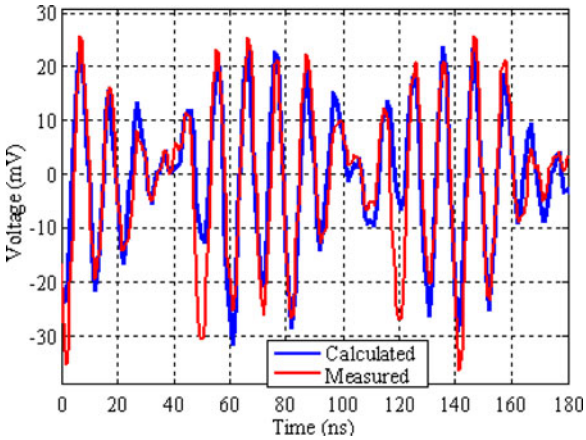

Fig. 16. Noise voltage waveform at port 1 when implementing the T-flip-flop design.

2.5, 5, and 10 MHz. These components were not driven by the implemented T-flip-flop circuit, but rather by other circuitry in the FPGA that were not considered in our simulation. Good agreement can also be seen between measured and simulated values in the time domain as shown in Fig. 16. Similar studies of the noise voltage at port 3 (the near port) also showed a good match between the measured and simulated results.

Fig. 17 compares measured and simulated noise voltages at port 1 when the FPGA implemented the gray code counter. In this case, the gray code counter consumed 40% of the available resources in the FPGA. Results were generated when there were no decoupling capacitors on the PCB. There was generally a very good comparison between the results except at very low frequencies (e.g., below 600 kHz). The high-frequency energy "spikes" are due to switching inside the FPGA, which is accurately accounted for by Quartus PPPA. The low-frequency components below 600 kHz are not due to switching of logic gates but are due to other noise sources that are not accounted for by Quartus PPPA. This low frequency noise caused a low frequency "wander" in the time-domain signal as shown in Fig. 17(b).

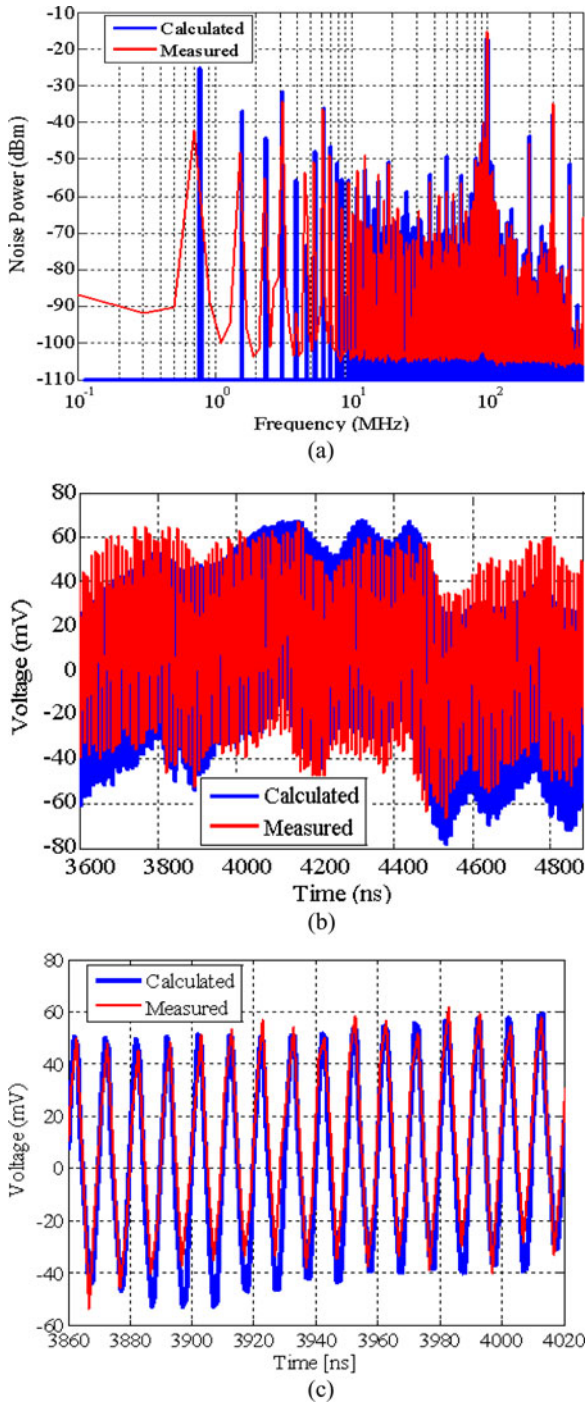

Fig. 17. Noise voltage at port 1 when implementing the gray code counter design, consuming 40% of FPGA resources (a) spectrum, (b) time-domain waveform, and (c) closeup of time-domain waveform.

None the less, there is a good comparison of the time-domain signals at high frequency, as indicated in Fig. 17(c).

Fig. 18 shows another comparison of measured and simulated noise voltages while implementing the gray code counter, except in this case all 16 decoupling capacitors were placed on the board. The measured and simulated noise voltages again match well.

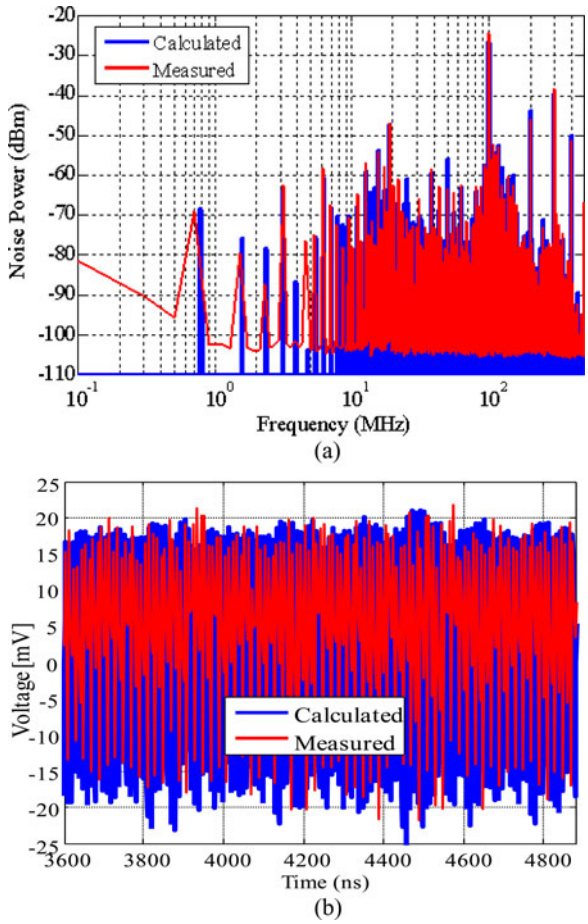

Fig. 18. Noise voltage at port 1 when implementing the gray code counter design consuming 40% of FPGA resources, and 16 decoupling capacitors were mounted on PCB. (a) Spectrum. (b) Time-domain waveform.

It is interesting to note the strong noise voltage at 100 and 300 MHz observed in Figs. 15, 17, and 18. The FPGA is stimulating resonances in the board at these frequencies, as illustrated in Figs. 10, 12, and 13. Controlling these resonances can be critical to power bus design—particularly in the case of an analog device with a narrow-band sensitivity to noise, where a slight shift in the resonance frequency or the quality of the resonance can have a significant impact on performance.

V. Conclusion

A methodology to estimate power supply noise associated with switching activity in an FPGA was proposed. Switching currents in the FPGA could be estimated by controlling the simulation time over which power analysis was performed. This technique has the advantage over traditional methods that no detailed information about the innerworkings of the FPGA is required beyond what is available in the FPGA simulation tool. The current waveforms can also be found relatively quickly with minimal computational resources. Lumped-element models were used to accurately represent the IC die and package up to 1 GHz, but a more sophisticated cavity-based model was required for the PCB to get accurate results up to that frequency. Once the PDN was constructed, the power supply noise can be estimated directly from the impedance network and the switching current. Good agreement between simulated and measured values of noise voltage on the PCB was found in both the time and frequency domains. This simulation approach can be used to more intelligently evaluate FPGA designs and decoupling strategies for their impact on power supply noise and the associated jitter and/or emissions it generates.

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