DAT110
Methods for Electronic System Design and Verification

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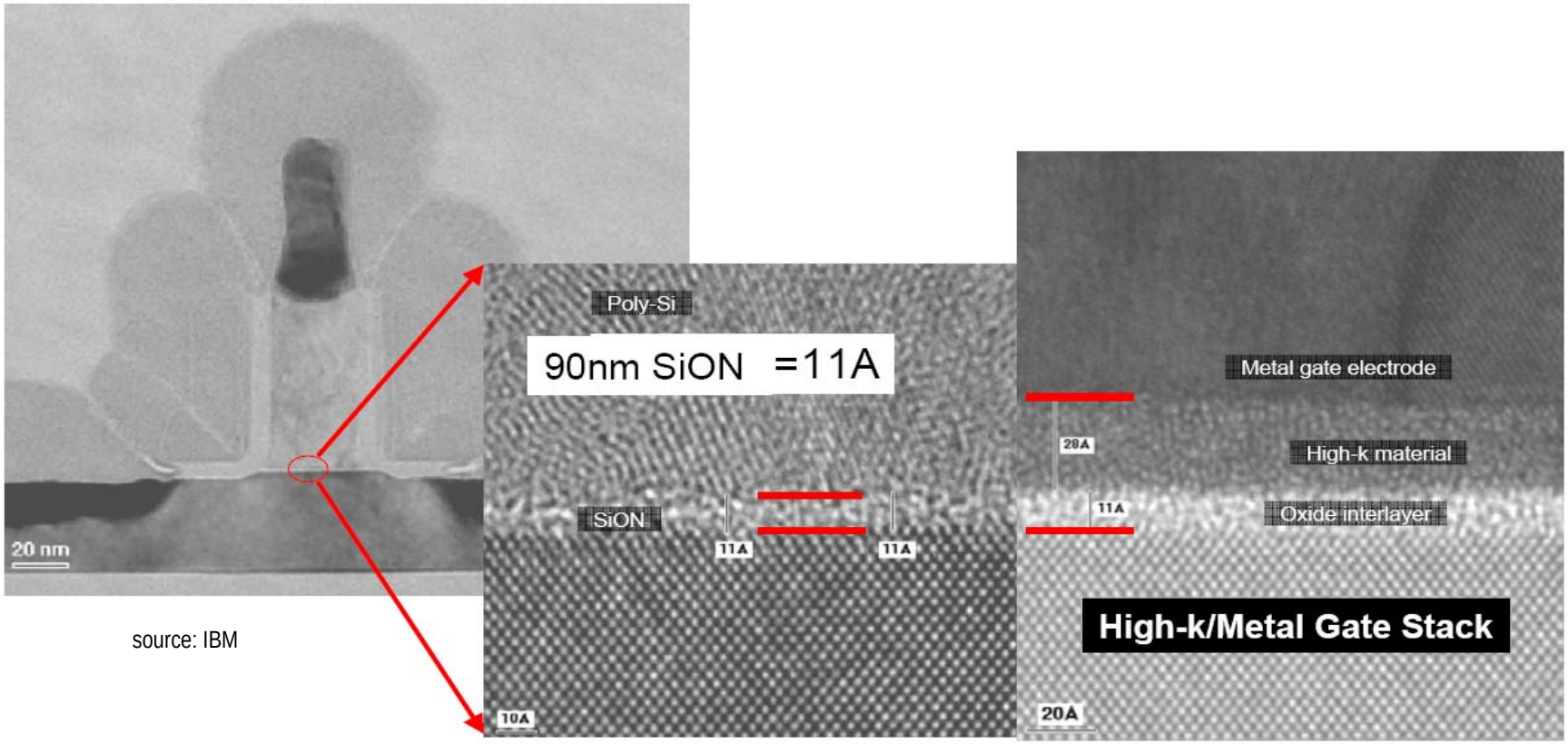
Lecture 8: Reliability and Test.

Device scaling and reliability

Scaled Transistors: Thin Oxides

- Consider insulator thickness: Silicon atom diameter is 0.26 nm.



source: IBM

90nm Gate Dielectric:
Tinv = 19A
ToxGL = 11A

High-k/Metal Gate Stack:
Tinv = 15.5A
ToxGL = 20A

The Oxide Tunneling Problem

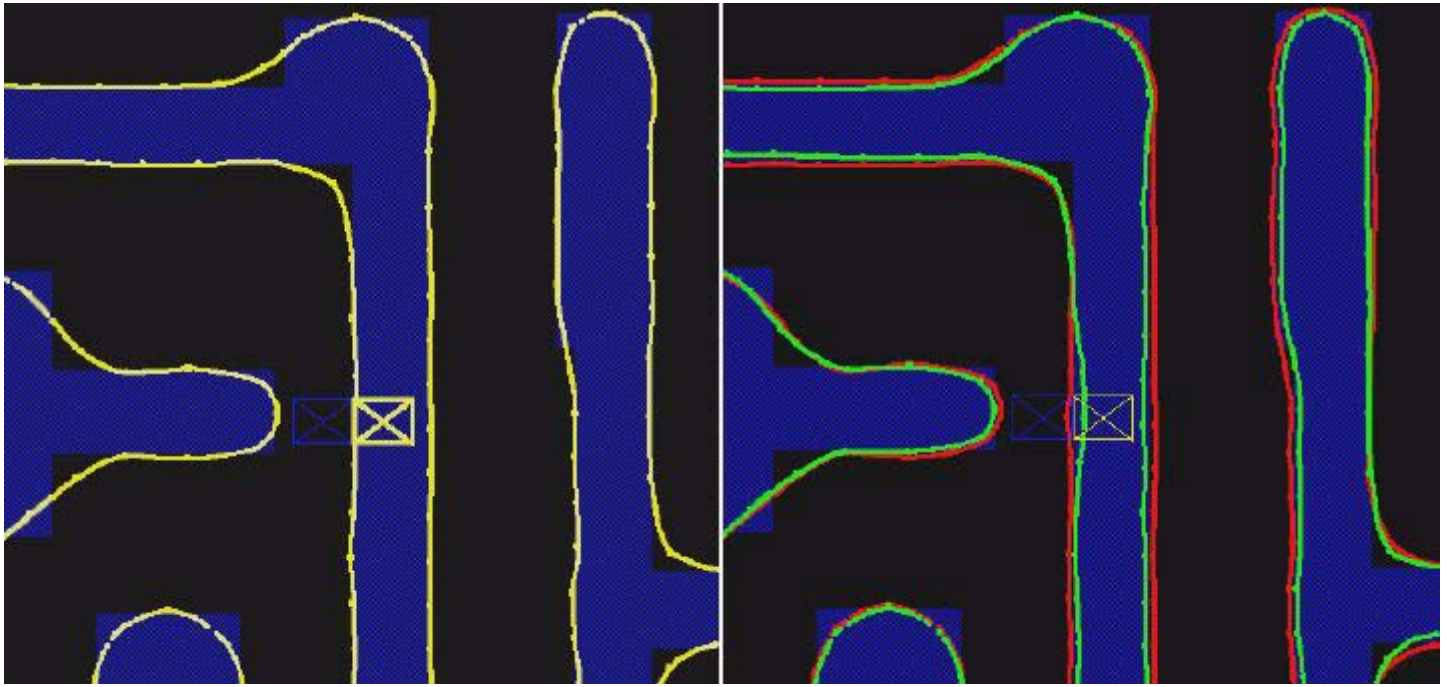
- High-*k* dielectric insulators enable
  a larger physical insulator thickness,
  without losing the gate's control of channel properties.
- A larger physical thickness reduces tunneling.
- Many high-*k* materials have been studied:
  - Aluminum oxide (Al_2O_3), titanium dioxide (TiO_2), tantalum pentoxide (Ta_2O_5), hafnium dioxide (HfO_2), hafnium silicate ($HfSiO_4$), zirconium oxide (ZrO_2), zirconium silicate ($ZrSiO_4$), lanthanum oxide (La_2O_3) ...
- Intel's 45-nm process: Hafnium-based insulator ($k \approx 25$).

Scaling Devices Makes Them Sensitive

- Thin oxides.
  - High electric fields across oxide $\Rightarrow$ the current punches through $\Rightarrow$ the insulating property is destroyed.
  - I/O transistors employ thick oxide.
- Thin and narrow wires.
  - Cannot carry large currents.
  - High resistance.

Layout Hotspots

- Hotspots: Specific patterns prone to bridging (shorts) or pinching (opens), as fabrication process drifts away from optimum condition.



Source: Roseboom

Trends

- Because of shrinking geometries, need for new terms:
  - Design For Manufacturing (DFM)
  - Design For Yield (DFY)
- Lithography using 193 nm light sources still common.
- TSMC intends to use extreme ultraviolet (EUV) for their 7-nm technology.
- Similar message from Samsung that intends to develop EUV-based 7-nm technology (EUV from ASML).

Failure mechanisms

What Can Go (Seriously) Wrong?

Apart from our own design mistakes, there are a number of catastrophic failures we may encounter:

- Catastrophic timing problems (hold violations).
- Power distribution problems (electromigration).
- Ageing problems (NBTI, HCI, TDDB).
- Thermal runaway problems (burn-in).
- Manufacturing problems in foundry/fab.
- *Single-event upsets could be considered for this list, but they are usually not catastrophic.*

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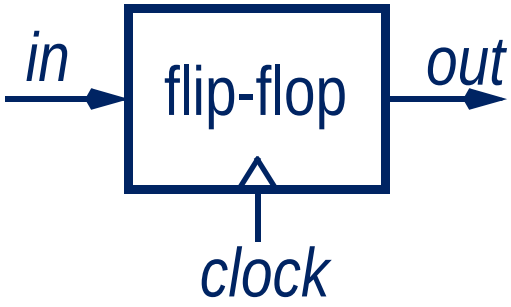
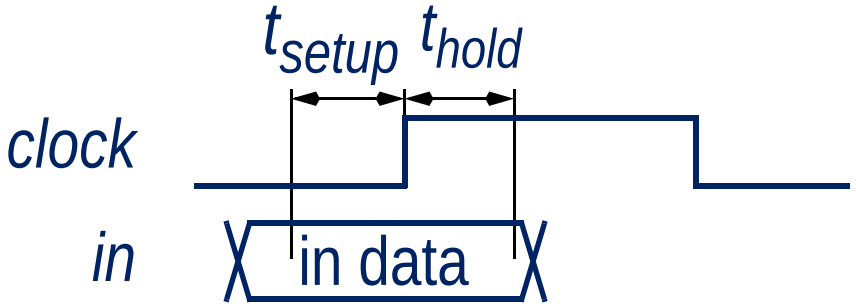
Repetition: Timing Properties of a Flip-Flop

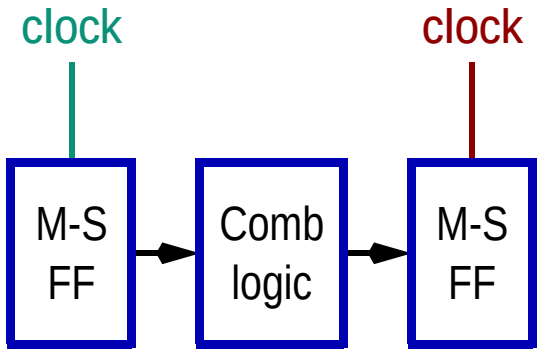
- Setup time/*hold time* is the minimal time before/*after* the clock edge that stable data needs to be available at the flip-flop input for functionality to be ensured.
- Recovery time/*removal time* is used for set and reset signals.

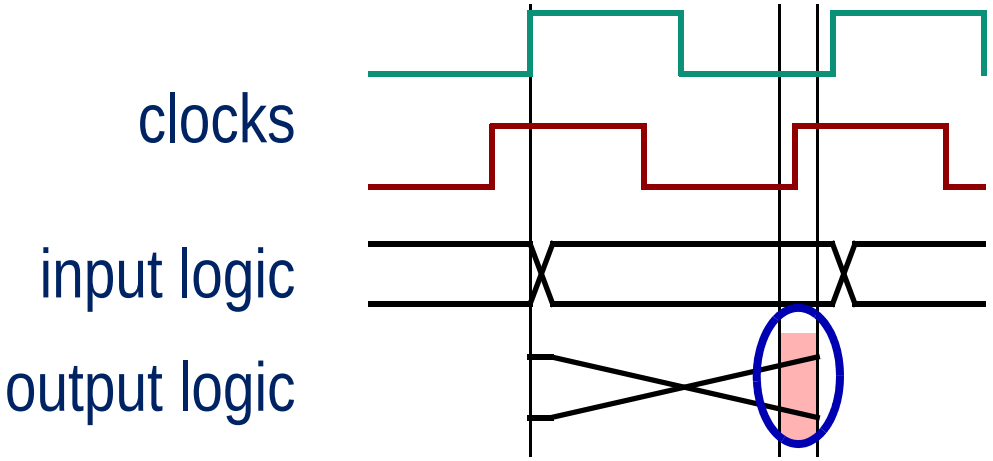




Negative Skew - Clock Flows Against Data

- Clock reaches capture FF before launch FF: Negative skew.
- Race cannot happen.

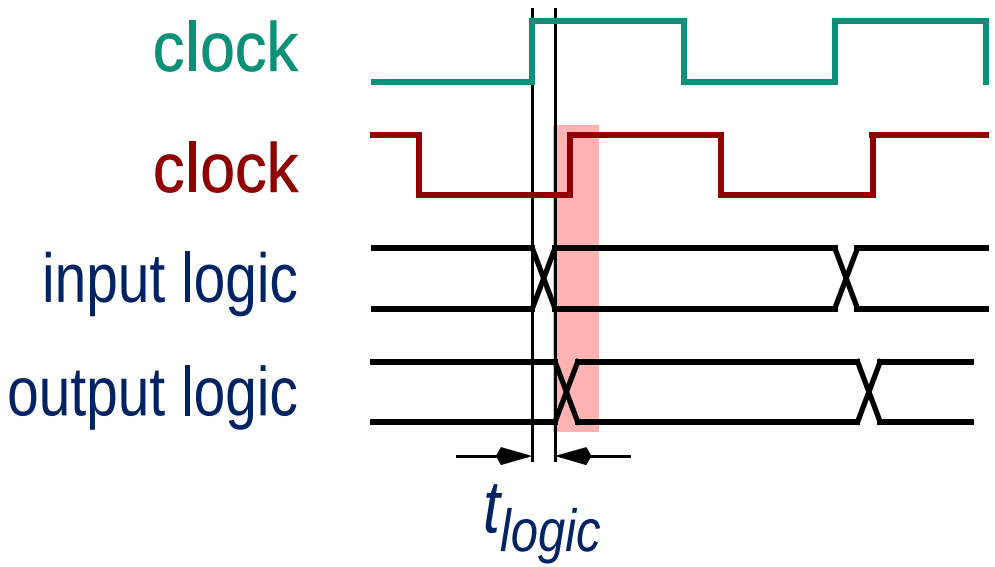




- Negative skew reduces the available evaluation time:
  We need to insert an extra design margin on the delay.
- If capture FF samples the wrong data, we have a setup violation.

Positive Skew - Clock Flows With Data

- Clock reaches capture FF after launch FF: Positive skew.
- If logic has very short delay, we may suffer from a hold violation (race).
- Hold violations could manifest inside shift registers or between FFs responsible for inter-block communication:
  - Cause of the latter: The respective clocks of the two blocks are produced in different clock trees and the relative skew is hard to control.



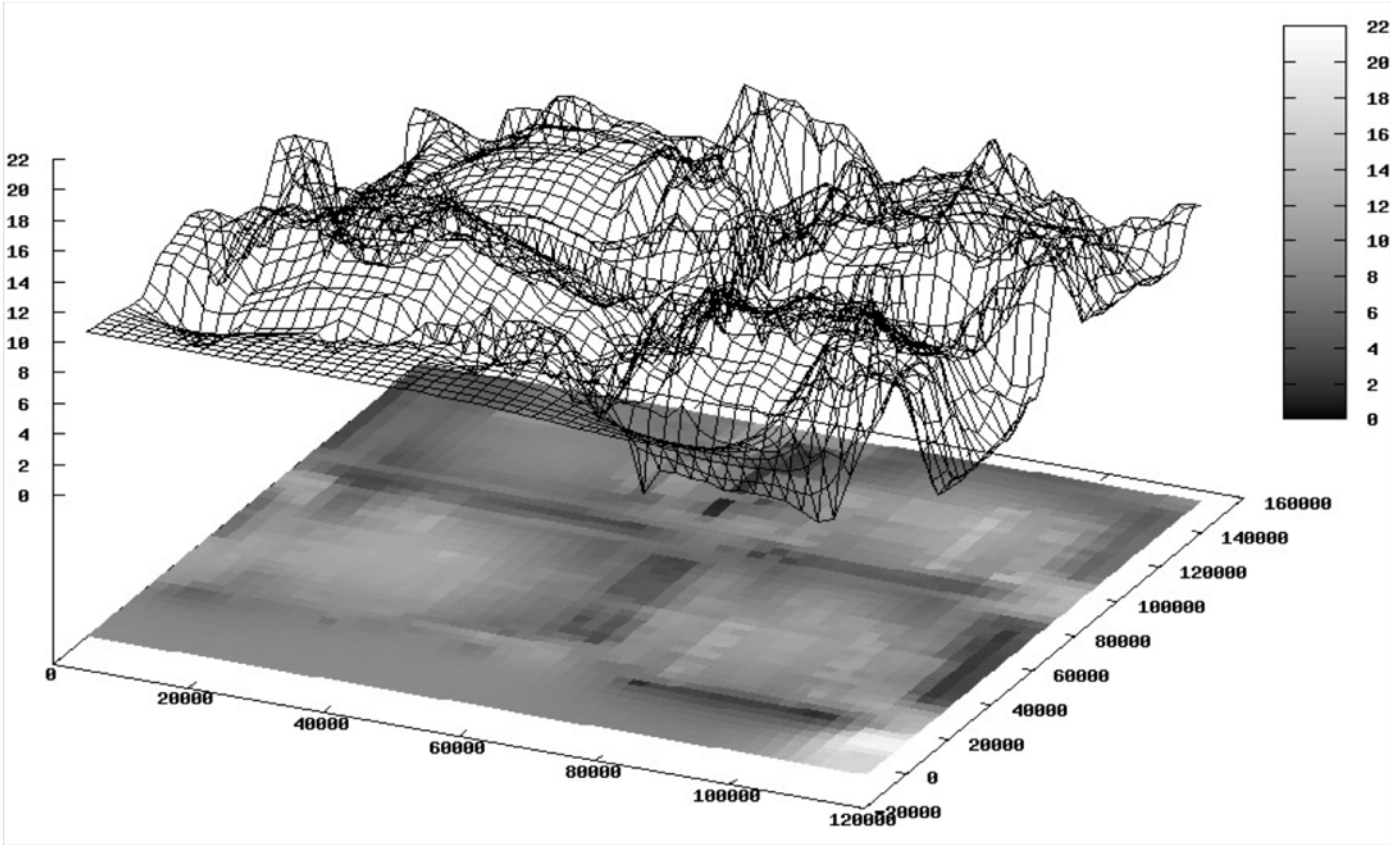
Unintentional Clock Skew Is Caused by ...

- Variation in effective channel length.
- Variation in threshold voltage V_T.
- Variation in ILD (inter-layer dielectric) thickness $\Rightarrow$ variation in C.
- Variation in supply voltage V_{DD}.
- Variation in temperature T.
- Signal coupling - crosstalk.
- Design choices, such as clock gating.

Comments on Positive and Negative Skew

- Negative clock skew.
  - Race can never happen.
  - Performance goes down. If you experience setup violations, reduce clock frequency to make the design work.
- Positive clock skew.
  - Race can happen.
  - If you experience hold violations
    your design is beyond recovery:
    Changing clock frequency does not help.

Timing Closure => Controlling Clock!

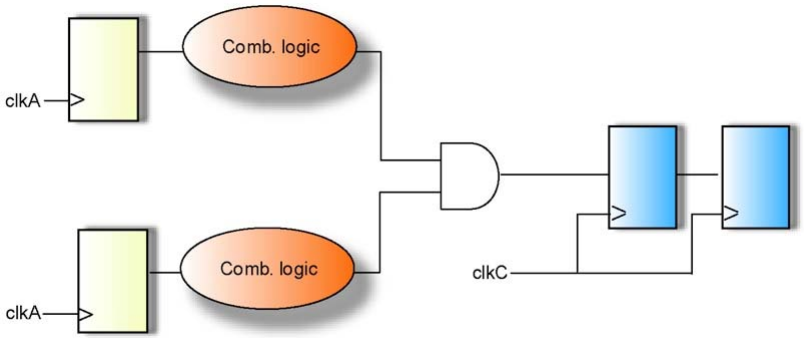


Source: AMD

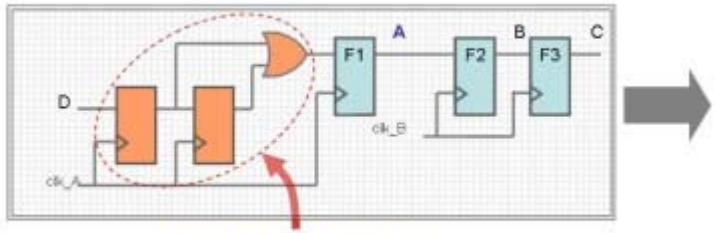
- Controlling the clock arrival at flip-flops is essential to synchronous behavior: Clock skew needs to be controlled.

Clock Domain Crossing (CDC) Issues

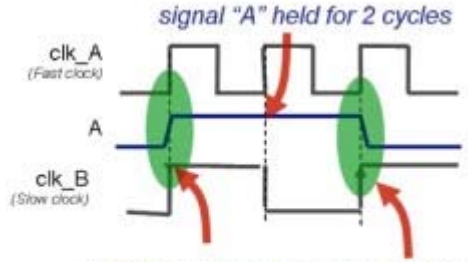
- Issues with e.g. cross-domain fan-ins: Rather synchronize first, then perform logic op:



- Issues with hold time violations on fast-to-slow clock crossings:



Simple 2-cycle Extender



Although data pulse at destination is full cycle wide, it may be lost due to Metastability effects

- Issues with Reset Domain Crossings (RDCs).

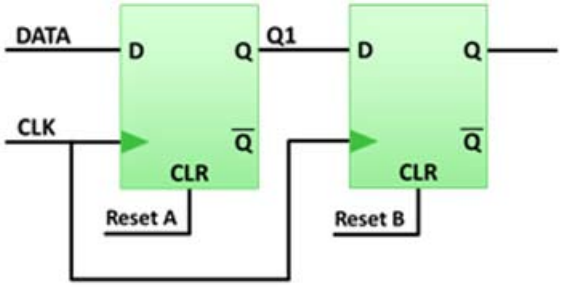


Figure 2a: Asynchronous Resets on Source and Destination Flop

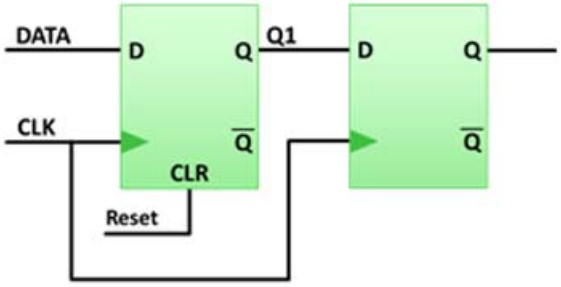


Figure 2b: Asynchronous Reset on Source Flop Only

Source: Synopsys/Atrenta (Spyglass).

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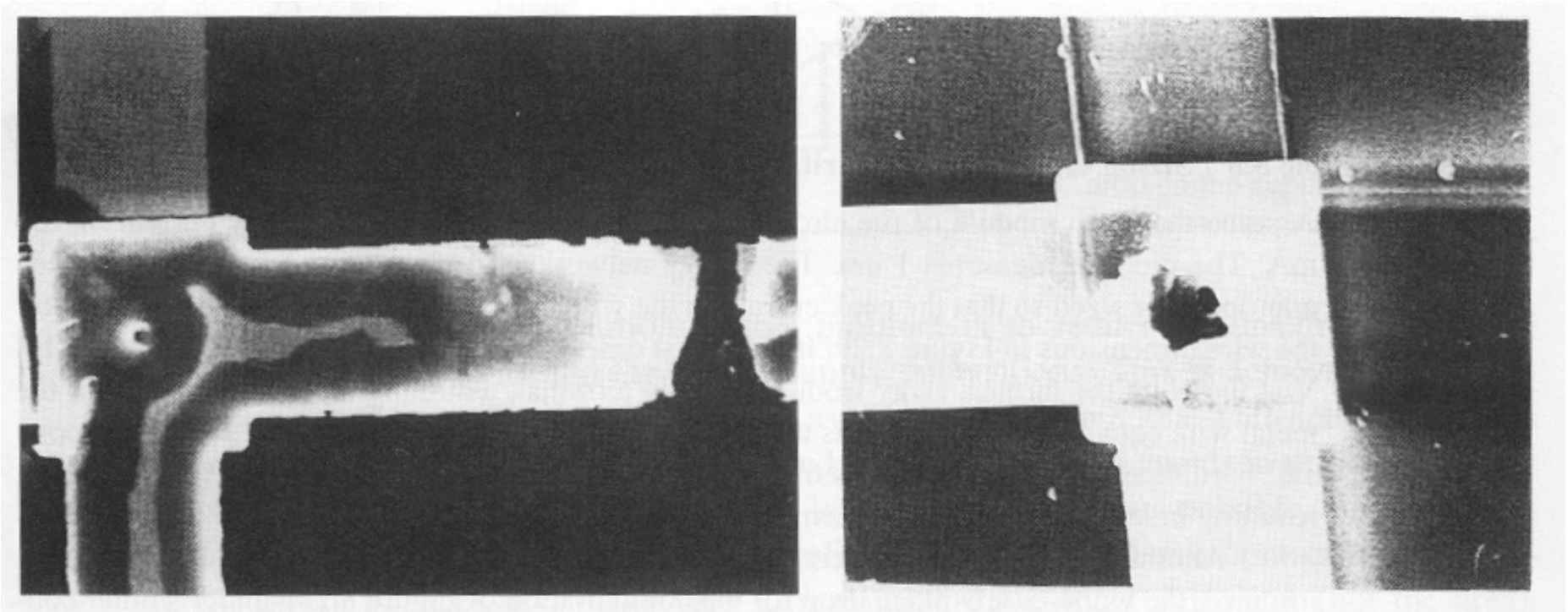
Power Rails and Electromigration

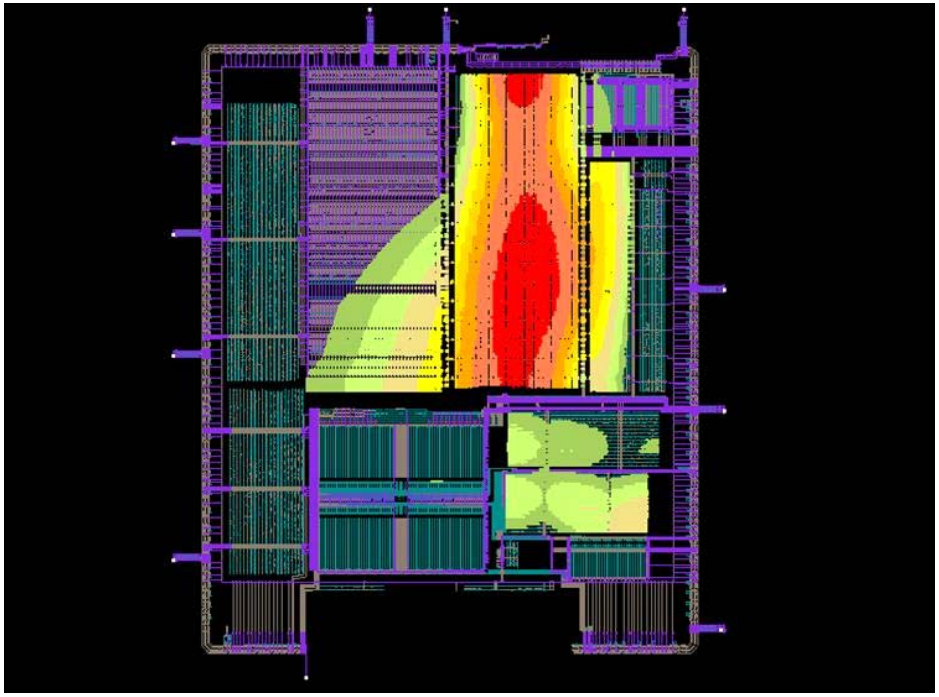
- When designing power rails for large circuits
  we must pay attention to the width of the wires [Lab exercise 4].
- Electromigration is the process of electric current
  moving metal atoms (ions) in the wires,
  making them break after some (quite long) time.
  - Especially 90° wire layout corners are sensitive.
- For AC rails (clock + signals) the effect of electromigration
  is an order of magnitude lower than for DC rails.
  - In scaled techs, signal wires can suffer from electromigration.
- Typical limiting DC value: 1.0 mA / μm width.

ELECTROMIGRATION



IR Drops

- As supply voltage wires get thinner and narrower, an increasing resistance gives rise to increasing voltage drops ⇒ gate delay increases.

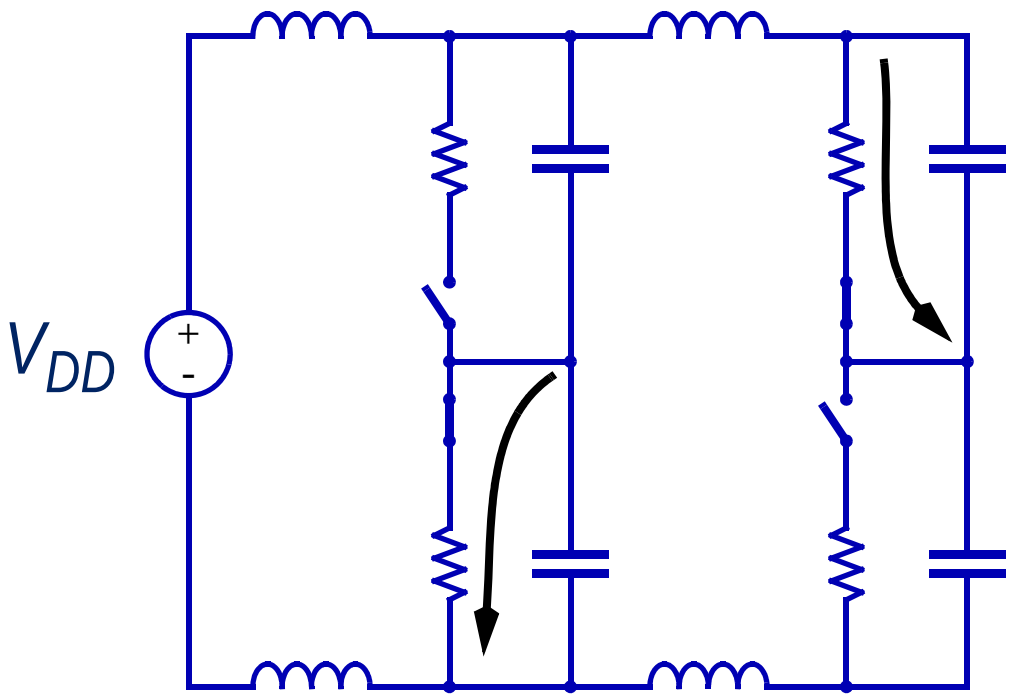


Source: Cadence.

dI/dt Noise

- Synchronous systems have high peak currents.
- The power rail network acts as inductance = low-pass filter.
- Power rail voltage will vary:

  $\Delta V = -L\frac{\mathrm{d}I}{\mathrm{d}t}$. This is known as switching (*dI/dt*) noise.

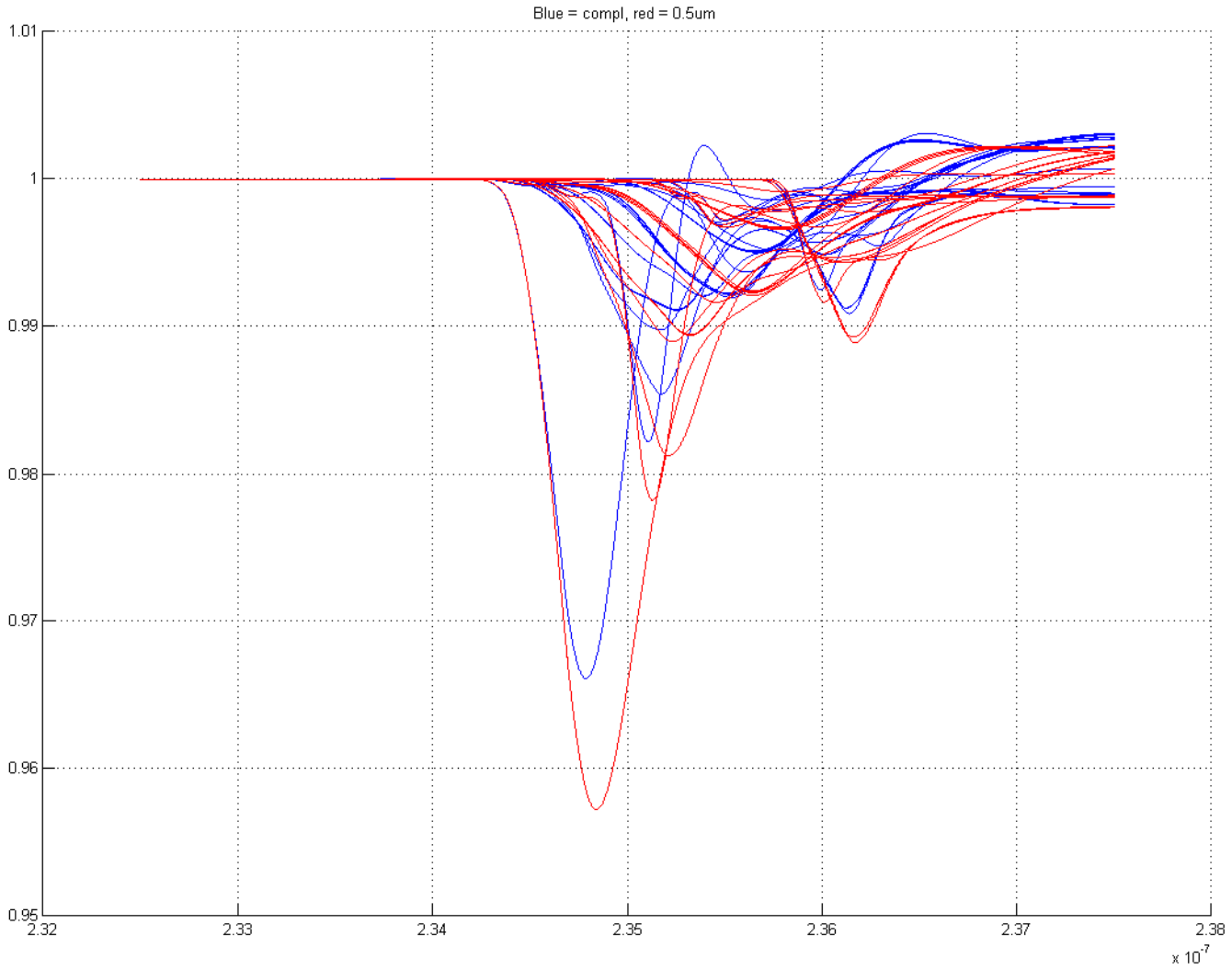


- Decoupling capacitances can somewhat mitigate the problem of switching noise.

Comments on Power Distribution

- Electromigration can lead to catastrophic failures, from which the chip cannot recover.
- IR drops and switching noise dynamically affect performance during the operation of a chip.

Simulation of Power Grid / Animation



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Negative Bias Temperature Instability

- NBTI = Negative Bias Temperature Instability
  makes a chip deteriorate over time.
- A gradual shift of threshold voltage over time in PMOSFET.
  NBTI gets worse ...
  - with scaling of transistor geometry.
  - as the electric field (V/m) across the insulator increases.
  - as average device temperatures generally increase.
- As supply voltages have been dropping,
  the threshold shift has come to have
  a relatively large impact on performance.

More on NBTI

- Origin: Interface traps exist between insulator and channel. Here holes can get stuck (when $V_{GS} < 0$ for PMOSFET).
- Interface states + fixed charges are both positive for the PMOSFET and thus results in a negative shift of threshold voltage.
  - In an NMOSFET, interface states and fixed charges are of different polarity. Therefore, they cancel each other.
- NBTI can cause immediate failures after burn-in.
- After burn-in the PMOSFETs may recover, but permanent damages that affect the ageing process are not uncommon.

Hot-Carrier Effect

- Also HCI = Hot Carrier Injection makes a chip deteriorate over time.
- "Hot" carriers have higher velocity than the thermal velocity, v_{th}:
  - $\frac{m \cdot v_{th}^2}{2} = \frac{kT}{2} \Rightarrow v_{th} = \sqrt{\frac{kT}{m}}$ for electrons.
- Hot carriers are drifting in high electric fields, around the drain terminal, when $|V_{DS}|$ is high.
  Shorter gate length yields higher HCI.
- 1) Hot carriers collide with crystal atoms,
  2) produce electron-hole pairs (impact ionization), after which
  3) electrons and holes penetrate and destroy insulators.

Time-Dependent Dielectric Breakdown

- TDDB = Time-Dependent Dielectric Breakdown
  wears out the gate insulator over time,
  leading to the formation of a conducting path to the substrate.
- High-quality insulators postpone the effect of TDDB.
- There is a trade off between
  gate insulator thickness and operating voltage specifications
  to achieve both speed and lifetime specifications.

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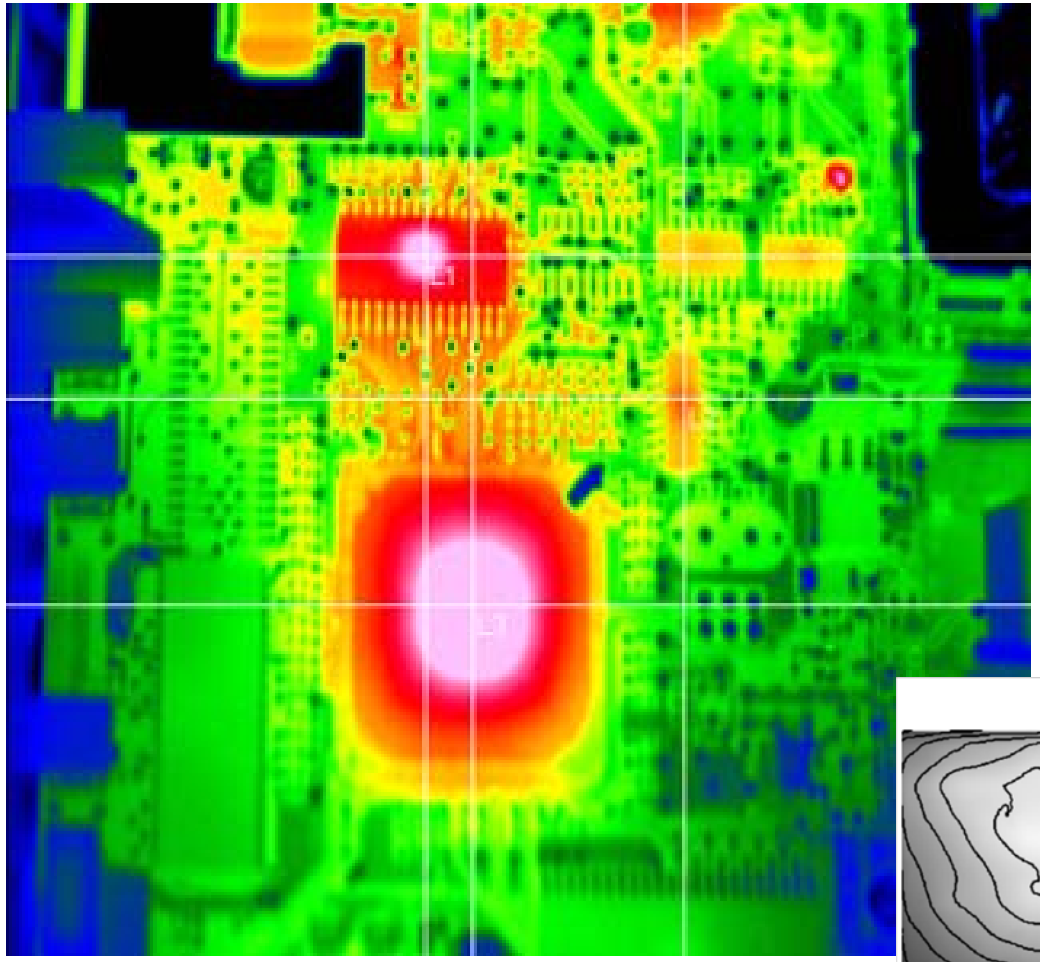
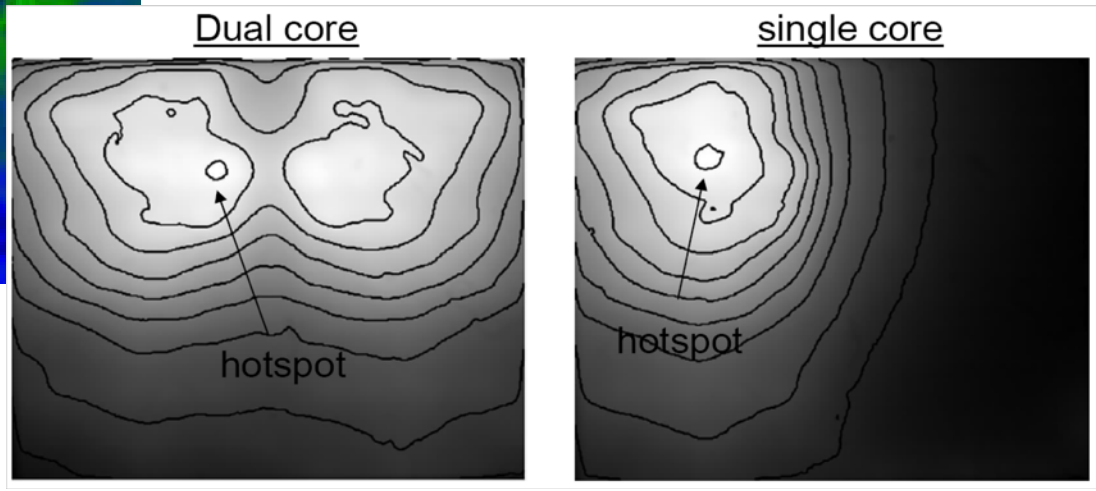
High Temperature Is Harmful



- Generally, high power dissipation leads to hot spots on boards and chips.
- Both absolute *T* and temperature gradients matter.

source: IBM



Chip Temperature

- Temperature is dependent on switching activity as well as leakage.
- Top temperatures can reach 110°C.
- Different areas of a chip may vary by ~40°C
  (memory is the coolest component).
- The die has a top passivation layer
  that acts as a “thermal blanket”;
  underneath there may be a thermal differential
  of as much as 45°C between
  the top metal layer and the silicon substrate.
- *More on burn-in later ...*

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Manufacturing Defects 1(2)

- Extra or missing materials.
  - Dust particles on the mask, wafer surface or processing chemicals, e.g. photoresist $\Rightarrow$ extra, unwanted material or unwanted etching of material.
- Gate Oxide Shorts (GOSs).
  - Pinhole defects are common thin-ox defects: Chemical contamination, nitride cracking at oxidation, crystal defects ...
  - *A GOS can be created in post-fabrication procedures and for some operational conditions: Electric field stress, ESD = Electro-Static Discharge, or through TDDB as we saw before.*

Manufacturing Defects 2(2)

- Shorting/bridging defects.
  - Shorts between signal/signal or signal/VDD or ground.
  - Gate-Oxide Shorts (*as mentioned earlier*).
  - Via punch-through, parasitic transistor leakage, defect pn junctions.
  - Bridging defects getting more common below 28 nm.
- Open defects (opens are more difficult to detect in CMOS circuits).
  - Missing conducting material or too much insulating material.
  - Faults can be time-dependent: Narrow opens can allow for tunneling. Coupling capacitance interactions and leakage currents can make an open appear something else.

Testing and debugging

The Wider Meaning of Testing and Debugging

- Testing.
  - Comprehensive and organized effort
    to exercise as many aspects as possible of an implementation
    for possible failure.
- Debugging.
  - Upon discovery of failure(s) = bug(s),
    the comprehensive and organized effort
    to close the existing bugs of an implementation.

Implementation and Production Flow

- Design-for-test (DFT) considerations (add dedicated test circuits).
  - Find test vectors that can find physical defects in a short amount of time.
- Acceptance testing.
  - Run pass/fail tests on manufactured chips.
  - Run parametric tests for performance on manufactured chips.
- Failure analysis.
  - Improve test coverage.
  - Improve design for next iteration.

Manufacturing Tests

- In electronics often test refers to the physical, experimental procedure of evaluating the manufactured hardware using e.g. pattern generators and logic analyzers.

Test-Vector Generation

- In order to develop a test strategy,
  models of physical defects are needed: Fault models ...
  - Stuck-at 0 fault, Stuck-at 1 fault, Bridging fault, etc.
- Fault simulation is used to find out how well
  a set of *p* test vectors can uncover defects
  in a circuit with *n* nodes.
  - Perform logic simulation; inject one fault at a time: $O(p\,n^2)$.
  - Fault simulation gives test vectors that have high test coverage.
- The automated process of finding efficient test vectors is called
  ATPG = Automatic Test Pattern Generation [D-algorithm, PODEM].

Testing Terminology 1(2)

- A defect is an unintended difference between the implemented/fabricated hardware and its intended function.
- An error is an erroneous response by a defective system.
- A fault is a logic-level abstraction of a physical defect.

Testing Terminology 2(2)

- Manufacturing tests (+ optional stress test).
  - Check for defects after fabrication steps.
  - Structural tests:
    Function is irrelevant, signatures like in logic BIST work fine.
- Functional tests.
  - Check and compare with desired (logic) functionality.
- Parametric tests.
  - Check and compare with desired performance
    (speed, power, robustness, etc.).
  - Scaling makes delay faults dominate physical defects (< 28nm).

Test and Yield

- For large, cutting-edge SoC/uP designs, very advanced IC processes are used.
- When a new IC process is introduced: Manufacturing errors are more probable and the yield is low.
  - Zero-yield test may happen for new chips.
- When the IC process has matured, yield has become high.

Stress Test

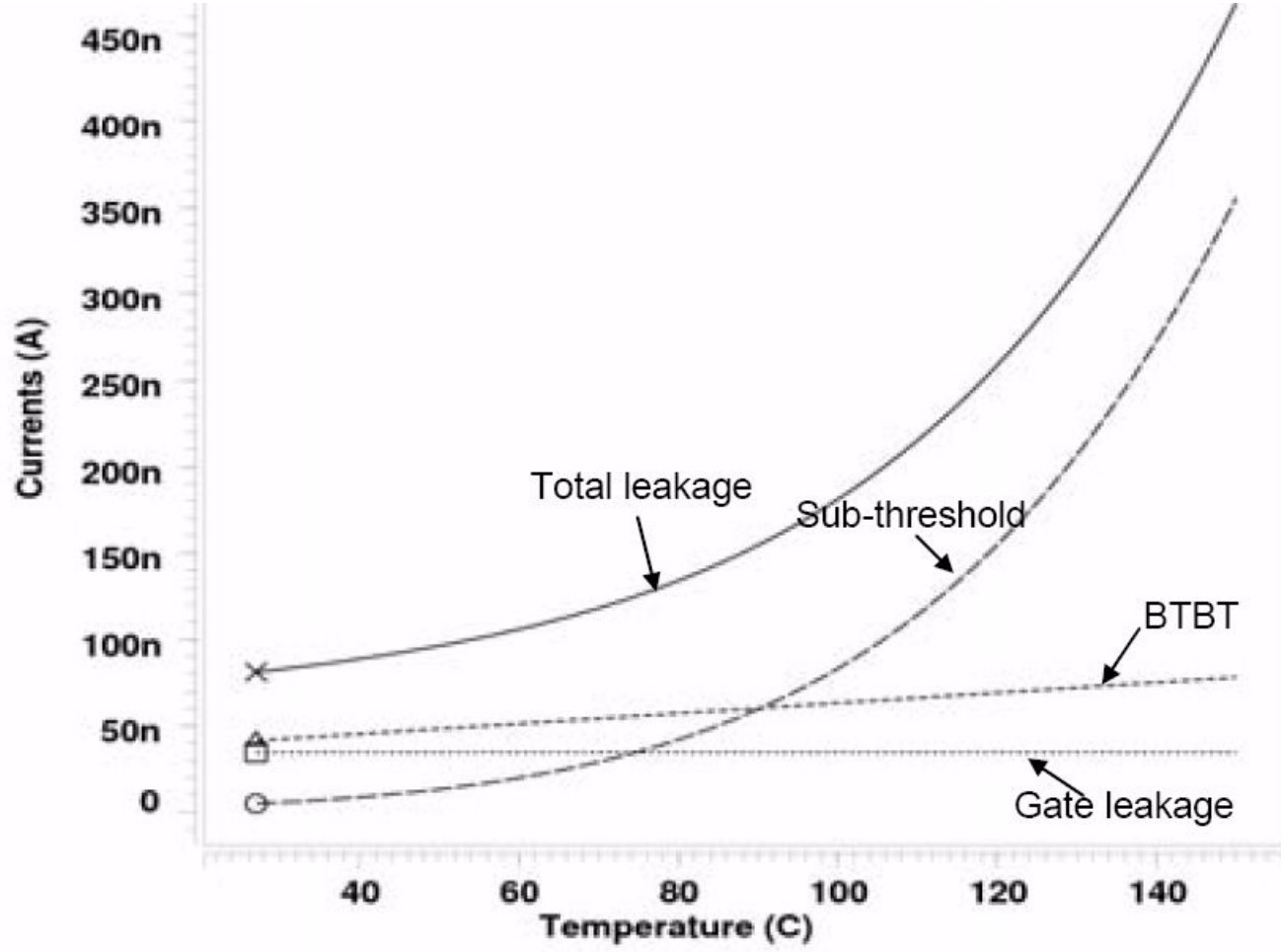
- In a stress test, extreme operating conditions are used; using cycling over large intervals.
  - In operating conditions, we include parameters such as temperature and mechanical stress.
- The stress test reveals how reliable a design is.
  - Poor parts are breaking down and only the good parts are leaving the fab/foundry.
  - Information on expected lifetime (Mean Time To Failure - MTTF) can be extracted.

The Burn-in Test

- Stress the chip by performing a burn-in procedure.
  - Static burn-in: Put IC in oven. Remove from oven. Retest.
  - Dynamic burn-in: Test at elevated temperatures...
    * Chip should be packaged and a subset of I/Os used.
    * Increase temperature to around 110°C.
    * Increase supply voltage to around 30% above nominal value.
  - NBTI for PMOSFETs may become a problem, and future ageing can accelerate.
- Now ... what happens if we happen to stress a chip, which has unusually low threshold voltages (due to variation)?

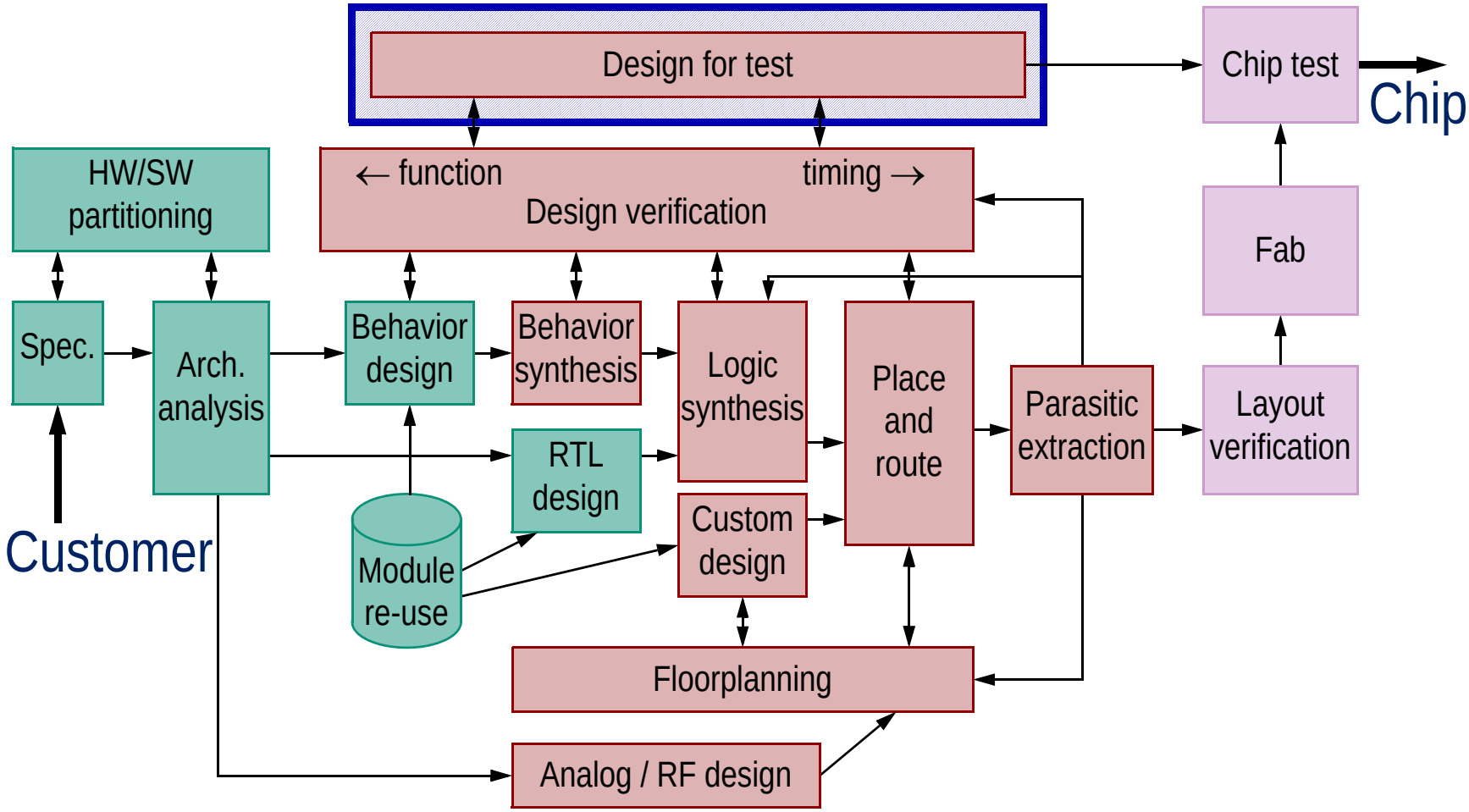
Burn-in Test Can Cause Thermal Runaway

Leakage increases
in hot areas
⇒
Increased leakage
heats the chip :-(
⇒
Heat can make
hardware malfunction
(or reduces
Mean Time To Failure)



Design For Test (DFT)

Present Scenario: Design For Test



Economy of Electronics

- The cost of fixing an error.
  - Fixing an error in initial design: cost ~ $10.
  - Fixing an error in layout: cost ~ $1000 - $500,000.
  - Fixing an error when reaching volume production:
    cost > $100,000,000
    (plus cost of replacing products = loss in precious goodwill).
- The cost of volume-oriented foundries/fabs.
  - Cost for a fab ~ $5,000,000,000 and rising!

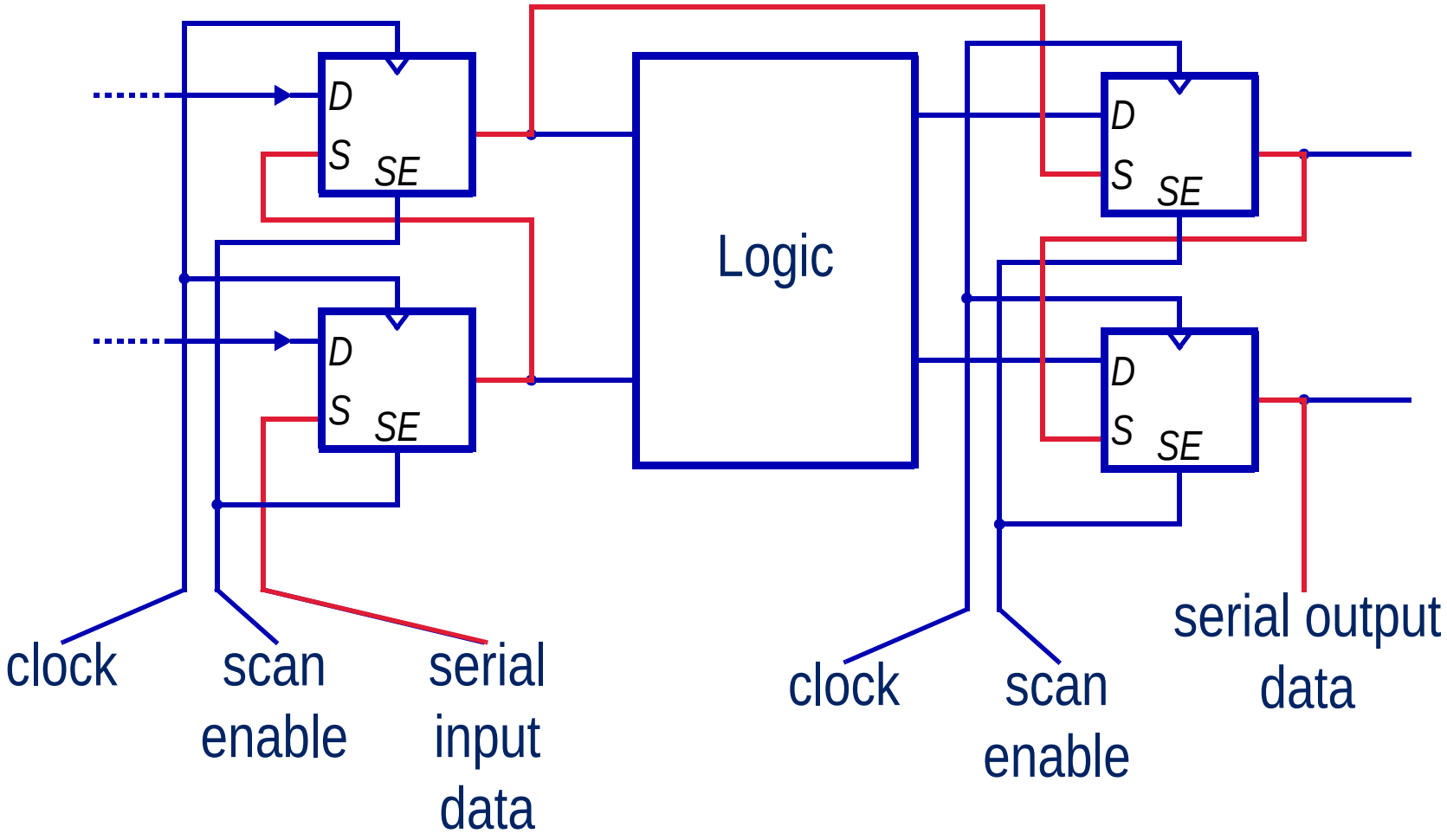
Design For Test (DFT)

- Test your manufactured design!
  - Failing designs cost short term (replacement/repair) and long term (goodwill).
  - Safety is a central issue in medical and vehicular equipment.
- Tests must be practical $\Rightarrow$
  Include hardware that
  enhances controllability and observability.
- Tests must be planned $\Rightarrow$
  A well-documented implementation makes test easier.

DFT Techniques

- *Ad hoc* testing: for example, test point insertion for observation.
- Scan-based testing.
  - Scan flip-flops connected in chains to allow test data to be moved in and out of logic core.
- Boundary scan - JTAG.
- Built In Self Test (BIST).
  - Pattern generators + response analyzers built into the logic.
  - Logic BIST (using scan chains).
  - Memory BIST: Built-in self repair (1D or 2D) can replace defect memory cells with spare cells.

Principle of Scan Chains



External or Internal Vector Generation?

- Traditionally scan chains are exercised using external ATPG-based automatic test equipment (ATE).
- To reduce test time, more I/O capacity is desired. But test cost is dominated by ATE, whose cost depends on I/O capacity $\Rightarrow$ What about internal tester?
- Logic BIST:
  - Pseudo-random pattern generators (PRPG) generate vectors, which are applied to scan chains, whose outputs are combined in a multi-input signature register (MISR).

Implementation Aspects

- ATPG: Specific faults + high test coverage + manufacturing tests.
  - needs vector decompression/compression to be scalable (since I/O capacity does not increase fast enough).
- Logic BIST: Fault agnostic + lower coverage + more suitable for system tests, power-on tests, etc.
- Scan chain infrastructure significantly impacts implementation:
  - Area overhead.
  - Scan reordering: Ensure each chain sits inside one Clk/VDD domain. Check potential hold time problems.
  - I/O pin count an issue. Pin sharing for logic and scan.

Other Challenges with ATPG-Based ATE

- Scan tests using ATPG-based ATE exercise registers more than regular operation does. Continuous at-speed testing not possible due to excessive power.
  - Use slow scan!
  - But slow scan means less vectors are tested per time unit.
- Even for slow scan, simultaneous switching (dI/dt) is a problem.
  - Use vectors with less switching activity $\Rightarrow$ extends test vector space by ~30%.
- At-speed testing using ATPG ATE is possible; use short bursts to reveal critical timing.

Other Challenges with BIST

- Due to the pseudo-random generation, BIST cannot as easily as external ATPG target specific faults.
  - Watch out for correlations:
    Choice of PRPG and seeds is important.

EDA Tools for DFT

- Siemens/Mentor.
  - acquired LogicVision.
  - offers Tessent Framework.
- Cadence.
  - Modus Test Solution.
- Synopsys DFT.
  - DFTMAX and TetraMAX.
- SynTest Technologies.
  - RobustScan and TurboBIST-Logic.

Reliability and Test: Conclusion

- Our hardware platform is getting less reliable.
  - IC device scaling is causing some reliability problems.
  - Changing operating conditions are causing other problems.
  - In total, a growing number of mechanisms have to be considered.
- Bottomline: We must test our electronic systems thoroughly!
- And to test our manufactured systems efficiently,
  we need to consider this test early,
  already during design / implementation.
- ATPG-based ATE vs logic BIST: Each has its role, strengths and weaknesses... but there is still a debate on which is “best”.