Course PM

DAT110, Methods for electronic system design and verification, 7.5 hec, Fall semester, 2018

Examiner: Per Larsson-Edefors
Course responsible: Per Larsson-Edefors
Lecturer technical writing: Anne Hsu Nilsson
TA: Christoffer Fougstedt and Erik Börjeson

Course content:

The lecture series, which mirrors the overall content of the course, covers: Terminology and structure of EDA systems. Design of electronic systems that are based on both software and hardware. Functional verification. Behavioral and logic synthesis. Timing analysis. Power and energy analysis. Physical design. Design for test and manufacturability. Discrete mathematics and optimization relevant to EDA. Technical writing.

Learning outcomes:

After completion of this course, the student should be able to

1. describe the algorithmic principles of a number of important EDA concepts, such as behavioral and logic synthesis, logic simulation, static timing analysis, timing closure and power dissipation analysis
2. describe contemporary EDA design flows and their fundamental weaknesses and strengths
3. apply Linux-based EDA tools, including simple shell scripts, for design and verification of digital electronic systems
4. perform timing-driven synthesis and power dissipation analysis for digital circuits
5. critically and systematically integrate knowledge, to model, simulate, and evaluate features of digital ASIC design flows
6. clearly and unambiguously communicate his/her conclusions of laboratory work and in-depth term paper studies, the knowledge and rationale underpinning these.

Course structure/course implementation:

The pedagogical concept of the course rests on three cornerstones:

- lectures: these mainly supply the design and verification context of advanced electronic systems containing software and hardware.
- lab exercises: these offer comprehensive hands-on training on industrially relevant design and verification problems using state-of-the-art EDA systems (from Cadence and Synopsys).
- term paper work: this gives the student an opportunity to study state-of-the-art research-level texts, which allows the student to focus on an appropriate and interesting technical area and at the same time obtain training in reading research papers and practice technical writing.

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Examination forms:

- Lab exercises in groups of two students on design flow, including synthesis and place-and-route for ASICs. 60% of grade is based on quality of preparation, VHDL handins, log books and lab report.
- Group work (3 students) on selected topics, including a term paper, oral presentation and opposition. 40% of grade is based on quality of term paper report and oral opposition.

Course literature:

Electronic Design Automation for Integrated Circuits Handbook - 2 Volume Set, by L. Lavagno, G. Martin, and L. Scheffer, CRC Press, 2006, ISBN 9780849330964.
(This book is also available from within Chalmers, as an electronic book.).

Electronic Design Automation for Integrated Circuits Handbook - 2 Volume Set, by Luciano Lavagno, Igor L. Markov, Grant E. Martin, Louis K. Scheffer, CRC Press, 2016, ISBN 9781482254501.

Schedule:

Lecture 1: Course information. Electronic system design and verification.
Lecture 2: Functional verification.
Lecture 3: Term paper information. Practical advice for lab exercises.
Lecture 4: Synthesis.
Lecture 5: Timing.
Lecture 6: Power and energy. Variability.
Lecture 7: Physical design.
Lecture 8: Reliability and test.
Lecture 9: Technical writing.
Lecture 10: Discrete mathematics and optimization strategies for EDA.
Workshop on term paper writing.
Term paper presentations.

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