CHALMERS
Department of Computer Science and Engineering

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DAT093
Introduction to Electronic System Design
Quick Start Tutorial on QuestaSim

Introduction

QuestaSim is a tool from the vendor Mentor Graphics for the simulation of electronic designs written in description languages like VHDL and Verilog. We will use QuestaSim but there is also a simplified version called ModelSim. For the things we do the two act the same. You can download a student edition of ModelSim from Mentors homepage and a version of ModelSim will be included if you download the Vivado WebPACK from Xilinx. Vivado is a complete tool from source file creation to FPGA download. Read more in Introduction to Vivado on the homepage.

The screen shots in this tutorial are taken from version 10.7a of QuestaSim and this is what´s installed in the labs. If you use another version of the tool there might be some slight changes in the GUI, but they are of no importance.

This quick start tutorial is in no way complete, but it will give you what you need for the introductory lab. We will look more closely at QuestaSim later on in the course. There is a more complete description called Introduction to QuestaSim on the homepage.

In the tool, you compile your design into code that QuestaSim can use for simulation and then run the simulation. The simulation can be run command by command from a command line but it´s much easier to do the simulation if we put the commands in a batch file, a so called do file, and run this file. Using this file will also mean that if we run the simulation several times it will always be the same simulation set that is run.

Another thing that can simplify the test is if we use test benches. A test bench is a top level design that uses your design as a component. The test bench assigns test stimuli to the inputs of your design and checks that the output signals from your design are as expected. In a simplified version the test bench just assigns input values and you will have to check the results at the outputs by yourself. For this to work you must make sure that the entity of your design exactly match the component declaration in the test bench. Stick to the descriptions in the lab assignments! If the entity and the component declaration don´t match then change your entity. **Don´t change the test bench!**

We will go through the process of simulating a design step by step, for now leaving out things that you don´t need right now.

Work flow

You start QuestaSim either from the start menu or by clicking on the icon  . QuestaSim will open up as seen in *Figure 1*.

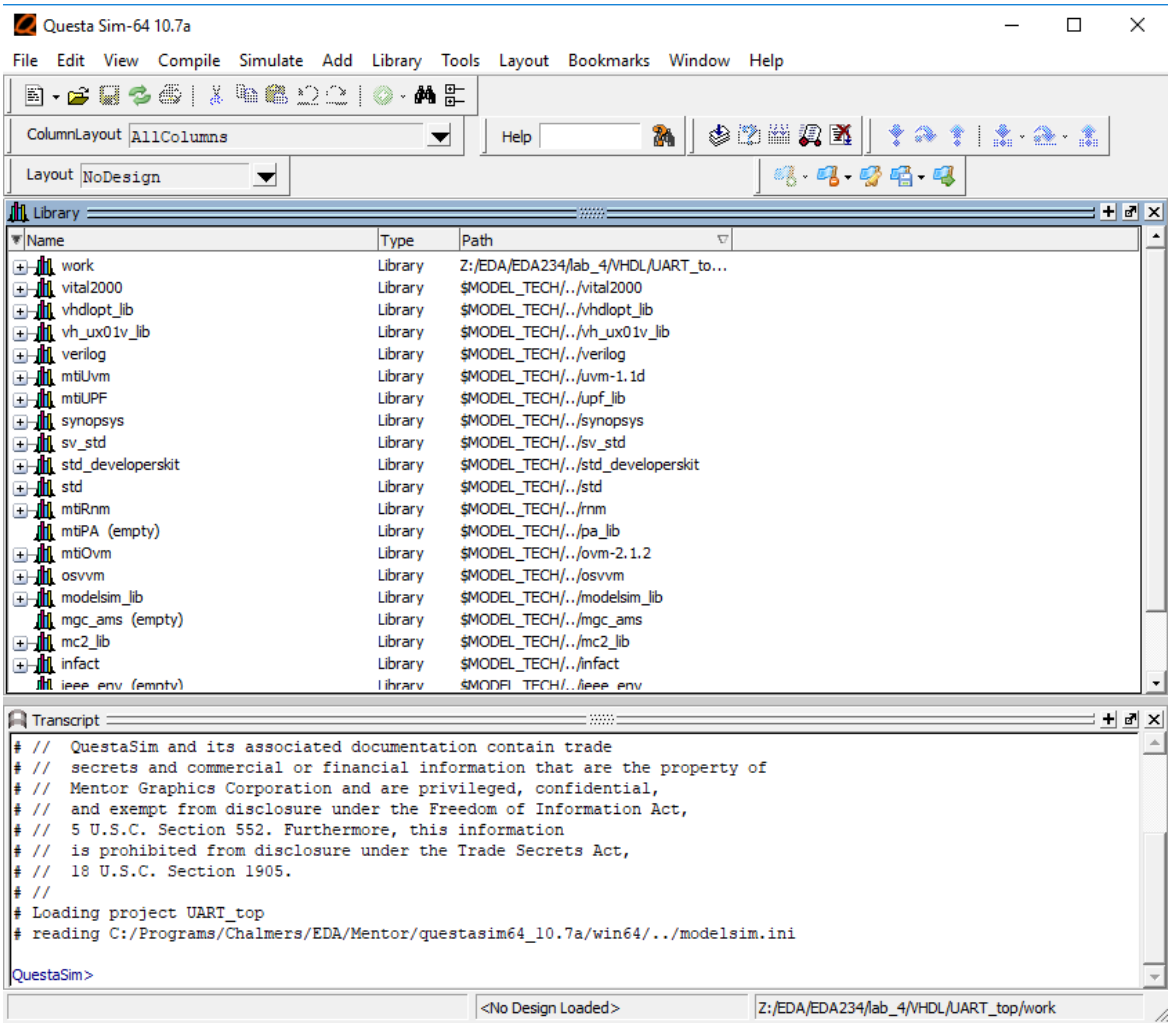


Figure 1 QuestaSim in start position

Setting up a project

The first thing you will do is create a new project. You create a new project by selecting File/New Project.. from the top menu and then you will get the dialogue in *Figure 2*.

By clicking on the Browse... button you get an ordinary file browser, *Figure 3*, where you can navigate to the folder where you want to store the project files.

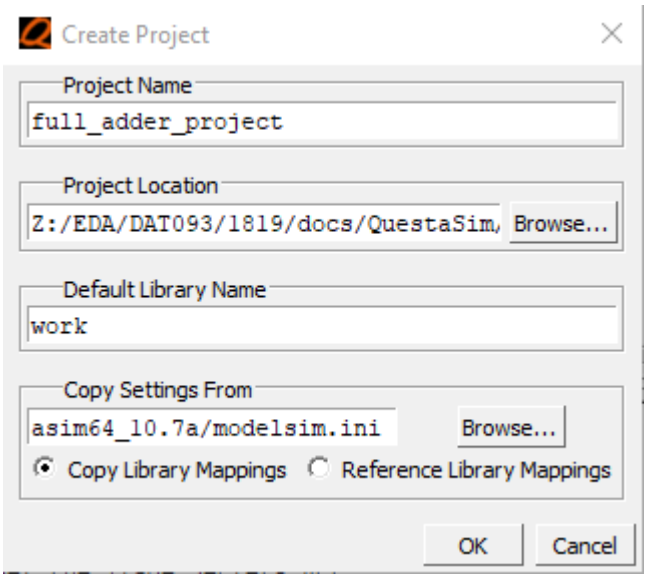


Figure 2 New Project dialogue

I like to keep things organized and put each project in its own folder. You don´t have to do this but I think it simplifies things.

To do this you can use the New folder button in the file browser to create a new folder for your design. You can also create the folder using an ordinary file browser before you start creating the project. I often find that easier. We will use a full adder as an example in this tutorial so we´ll create a project folder called `full_adder_project`.

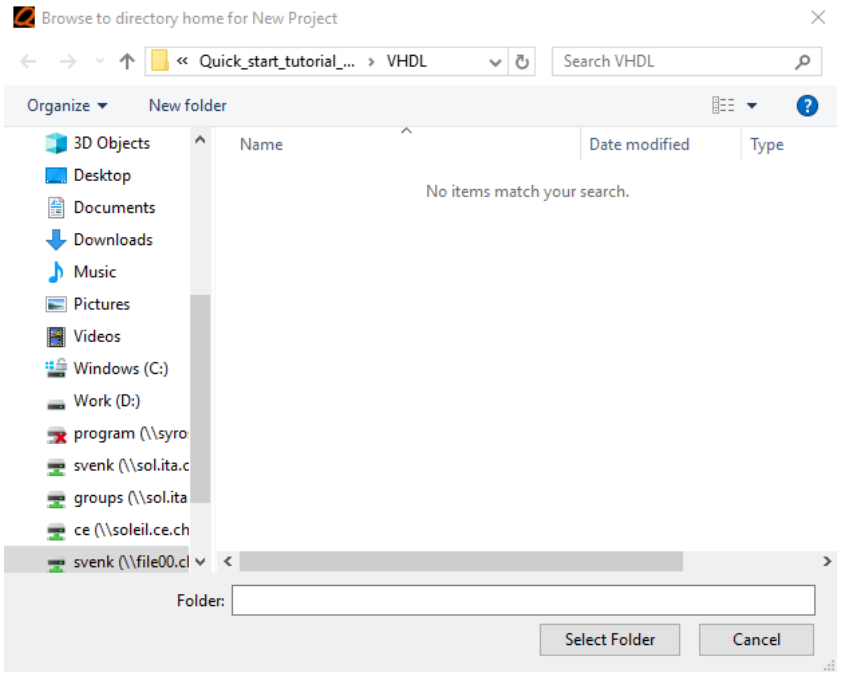


Figure 3 Folder dialogue

We continue by giving the project a name. To make things simple I prefer to use the same name for the project as the name of the folder where it´s placed.

When you click 

you will get the dialogue in *Figure 4* where you can either create new files or add already written files to your design. The files don´t have to be placed in the project folder. You can reference anywhere. This means that when you use old designs as components in your new design you don´t have to copy their files to the new project but leave them where they are. In that way, you don´t have to keep track of two versions of the file. Just be aware that by doing this, any edits will influence both projects.

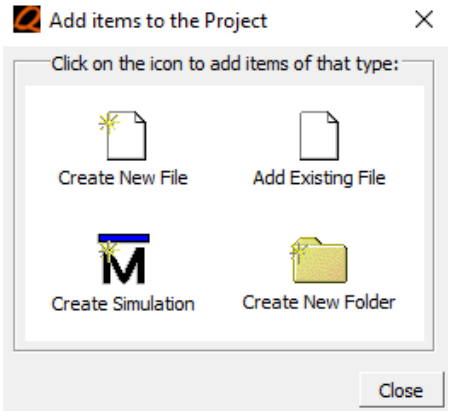
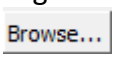


Figure 4 New/add file dialogue

You click on 

to add files and get the dialogue in *Figure 5*. You click on 

and get the file dialogue in *Figure 6*.

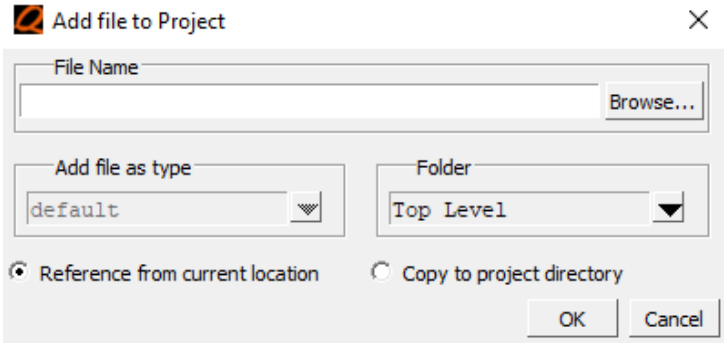


Figure 5 Add file dialogue

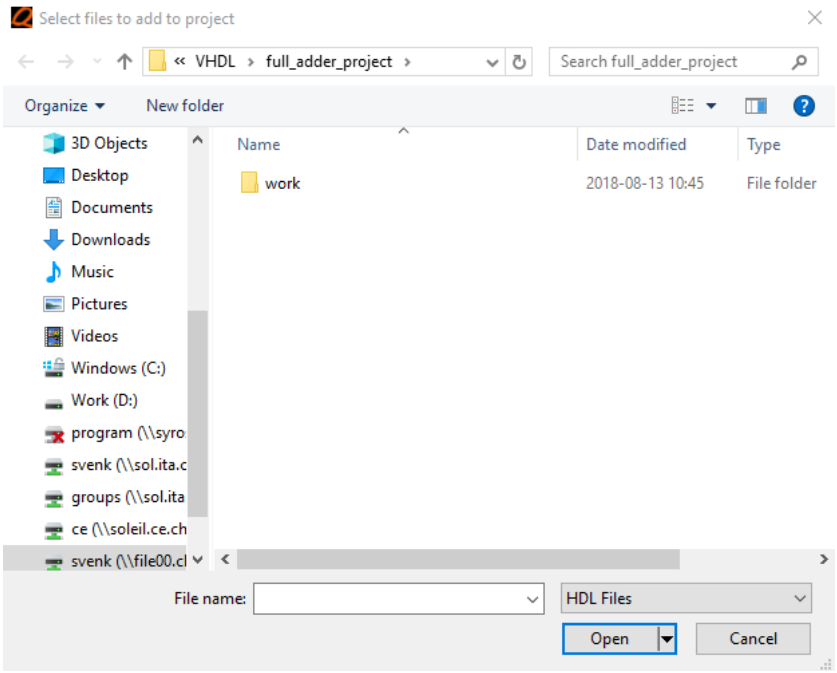


Figure 6 Add file browser

The browser is very similar to *Figure 3* but with an added file filter HDL Files so you can select what type of files to see in the browser. By default, the filter´s set to HDL files meaning VHDL and Verilog files. Later on we will add simulation script files called do files. These have no dedicated filter setting so to see them you will have to select All Files.

You can also use this dialogue to open an already created project. You should then change the file filer to Project Files and navigate to the project. The project file has a `.mpf` ending.

If you want to add files later on you can just right click in the Project window and select Add to Project/Existing File... or New File… and navigate to the file.

In *Figure 7* you can see the project when I have added the design, the test bench and the do file for the full adder. It is not necessary to add the do file to the project but if you do it´s easy to access and you just double click to open it for editing.

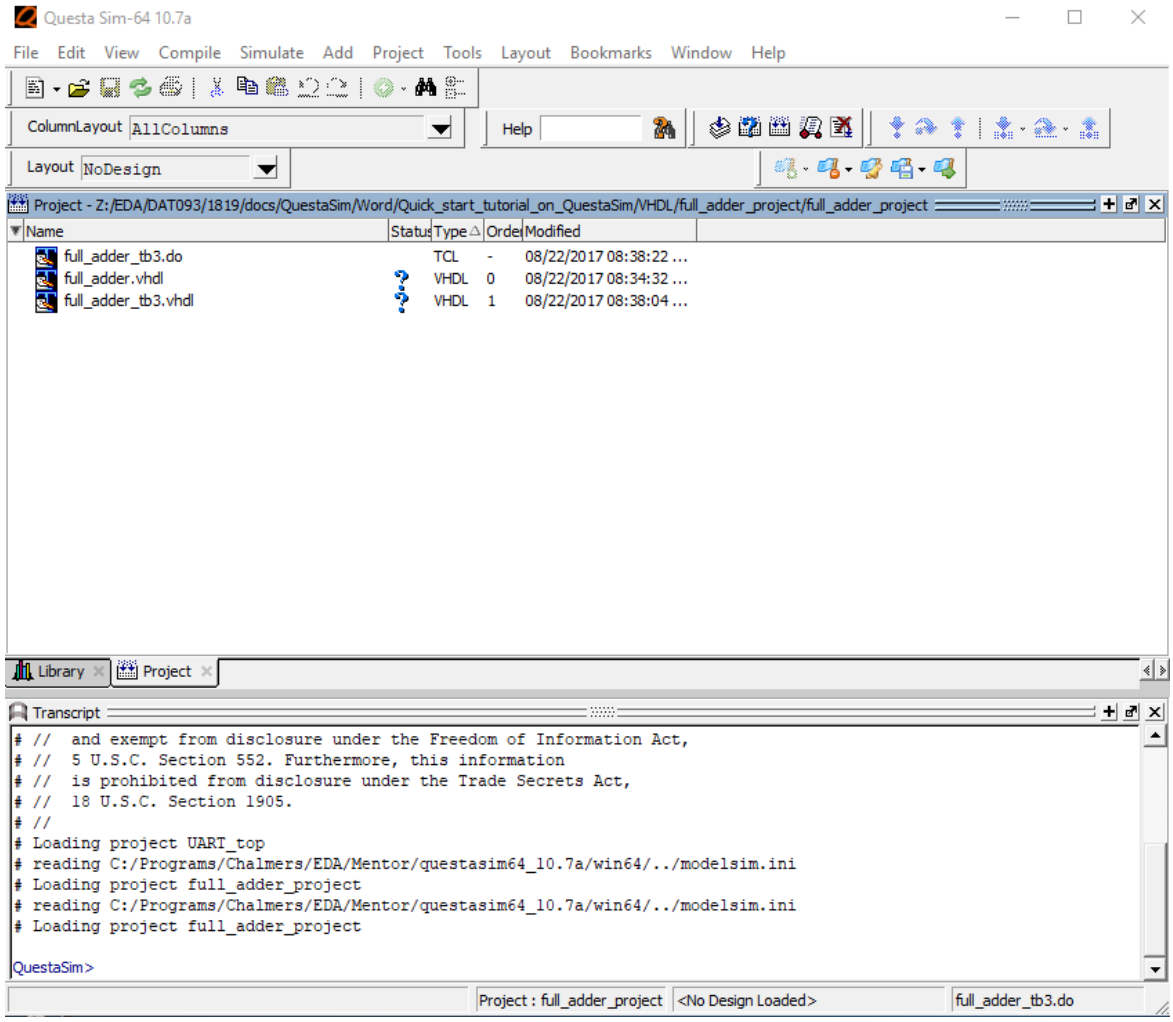


Figure 7 QuestaSim with an open project

The question marks on the VHDL file lines indicates that these files haven´t been compiled yet.

Compiling the project files

You can either compile one file by right clicking on the file name and select Compile/Compile Selected or compile all VHDL files by right clicking somewhere else in the Project window and select Compile/Compile All. Components that are used in a top-level design must be compiled before the top-level design is compiled. To do get the compilations I that order you can right click in the Project window and select Compile/Compile Order… and use the popup window to decide the order of compilation.

When you have compiled all files and if the files were without errors then you will get green markers on the files and green text in the Transcript window

```
# Compile of full_adder.vhdl was successful.
# Compile of full_adder_tb3.vhdl was successful.
```

indicating that you have been successful, *Figure 8*.

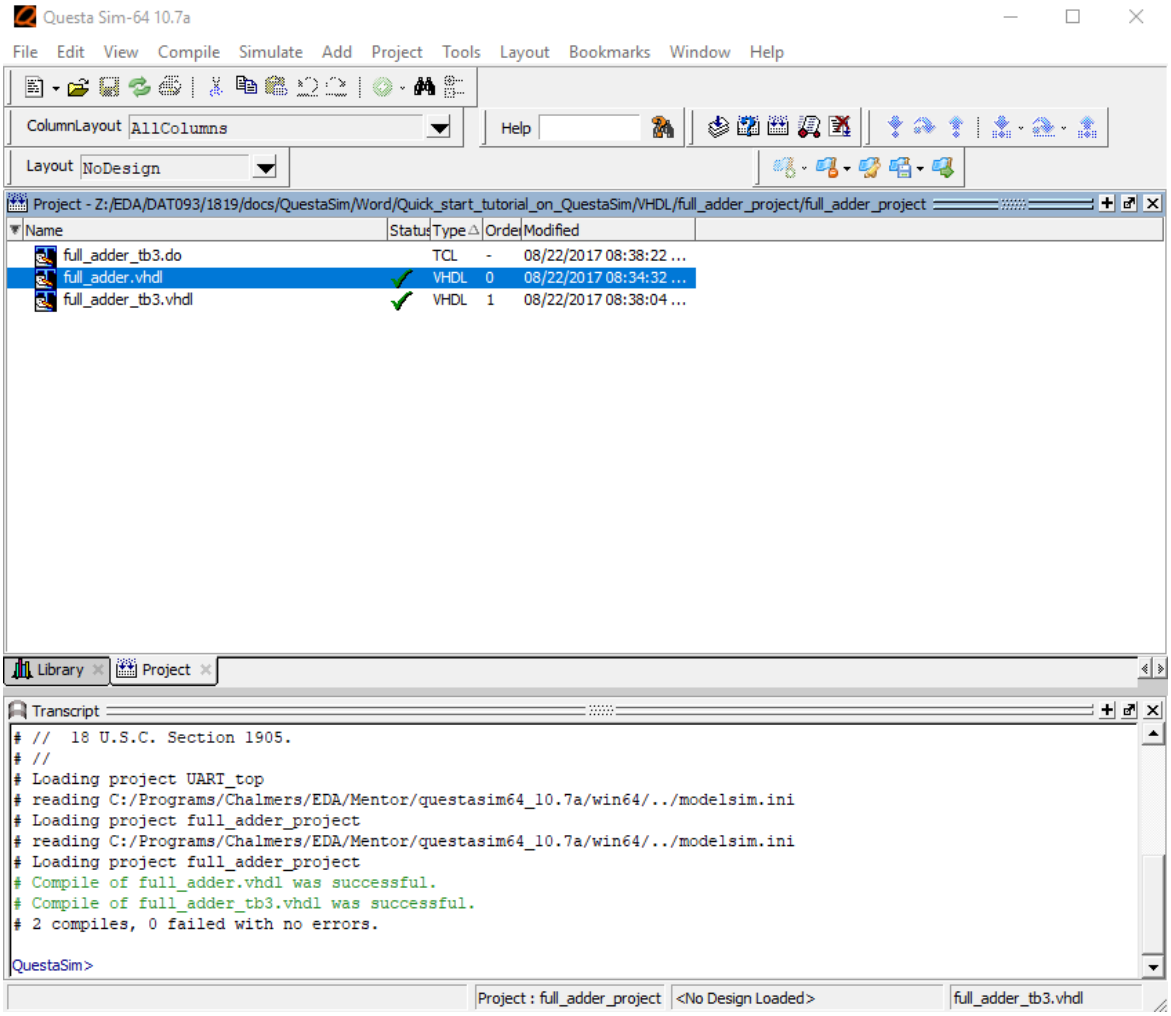


Figure 8 QuestaSim with successfully compiled files

If you weren´t that successful then the file containing the error(s) will have a red marker and you will get an error message, marked in red, in the Transcript window, *Figure 9*.

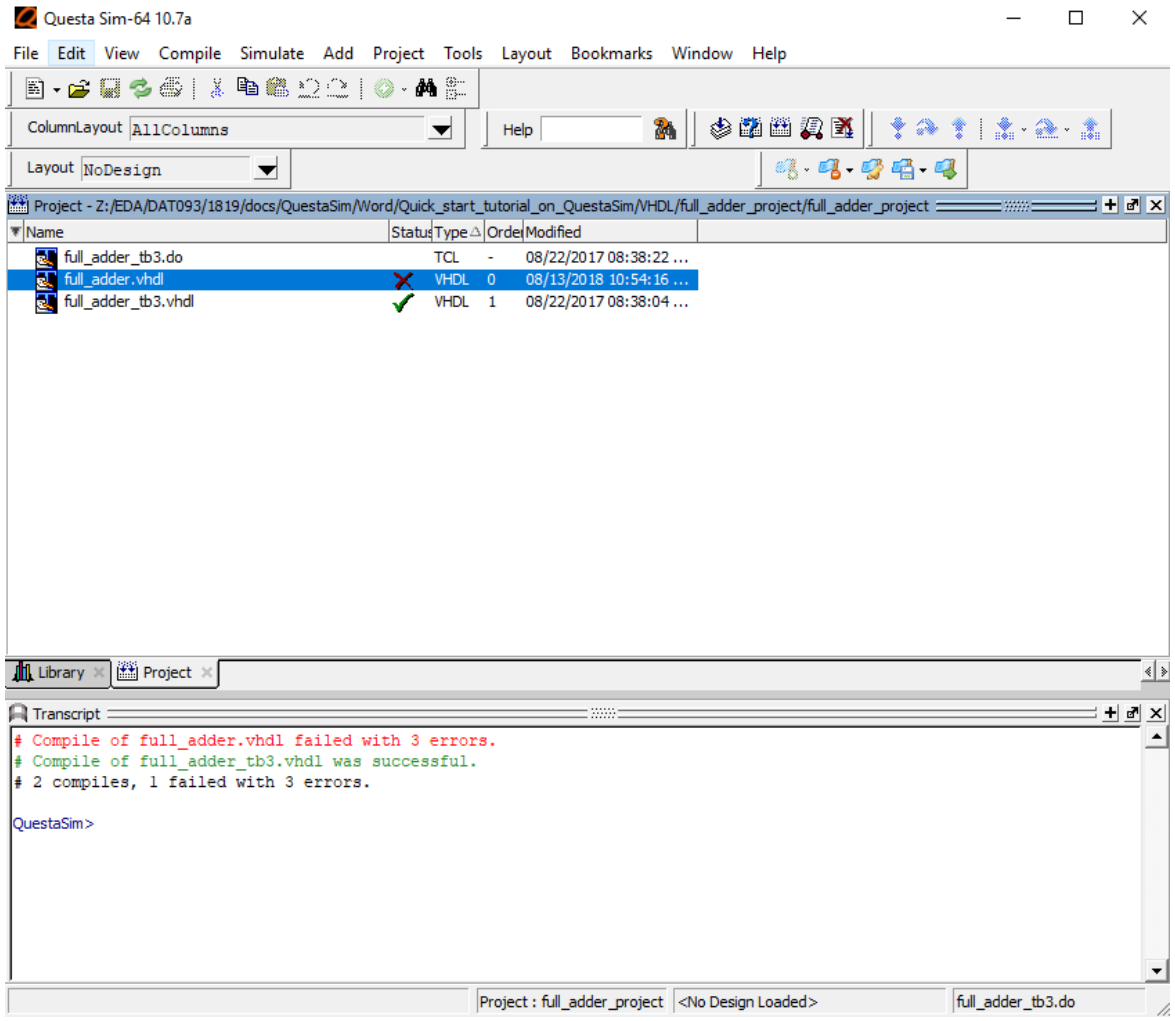


Figure 9 QuestaSim with an unsuccessfully compiled file

Don´t get discouraged if you get many errors. One error might lead to a number of another errors and fixing one of the errors might fix many or all of the errors.

To know more about the error(s) you double click on the red error message to get a list of the errors, *Figure 10*.

If you continue and double click on one of these error messages a text editor with the VHDL file will show and the incorrect line will be highlighted. In many cases it´s not the highlighted line that has an error but the actual error is just above that line in the code. In the example in *Figure 11* the message says that there is an error on line 12 but the error is actually a missing semicolon on line 11, the line above the highlighted line. You will find that it´s a very common situation that the error is above the highlighted line. The compiler won´t know there´s an error until it gets to the line after the incorrect line. Start from the top and work through the errors in the list. Correct one error, recompile and if you still have errors then do this process all over again.

When all the errors are corrected it´s time to start the simulation.

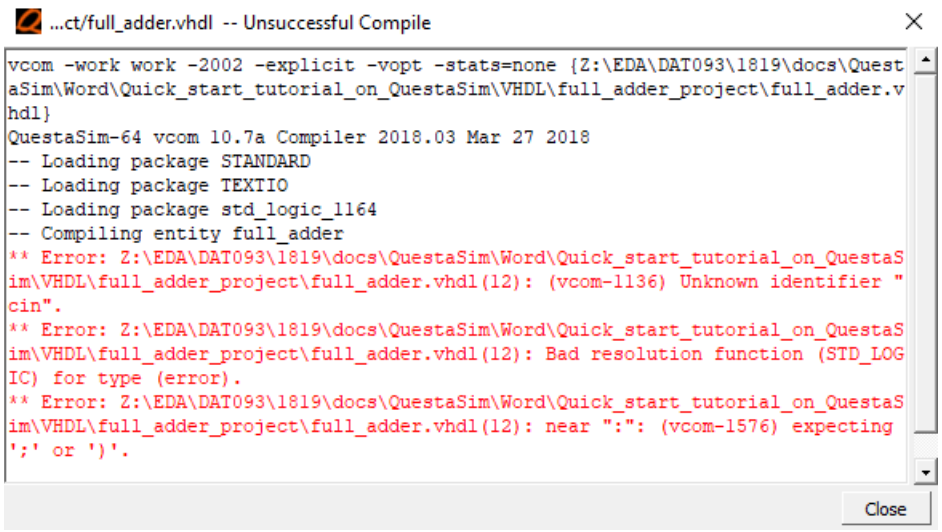


Figure 10 Error messages

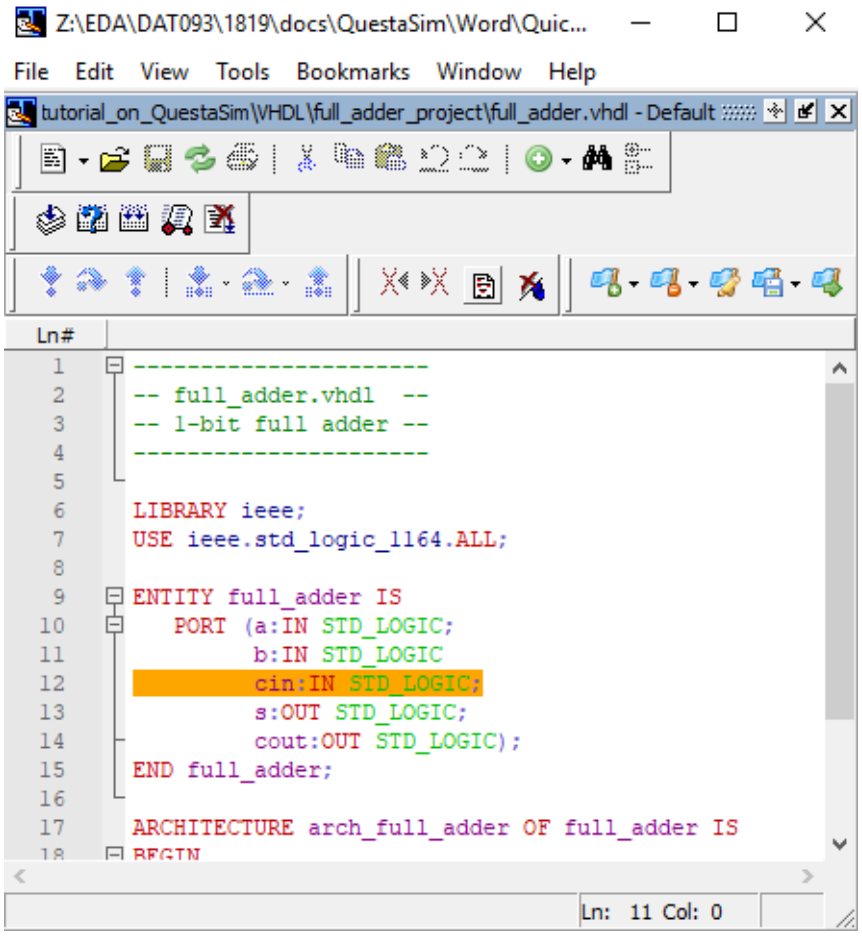


Figure 11 Highlighted error

Simulating the project

To start the simulation, you do the menu selection Simulate/Start Simulation… You´ll get the dialogue in *Figure 10*, where you select what to simulate. The compiled designs will be in the work library so open that folder and select the top-level design, in this case

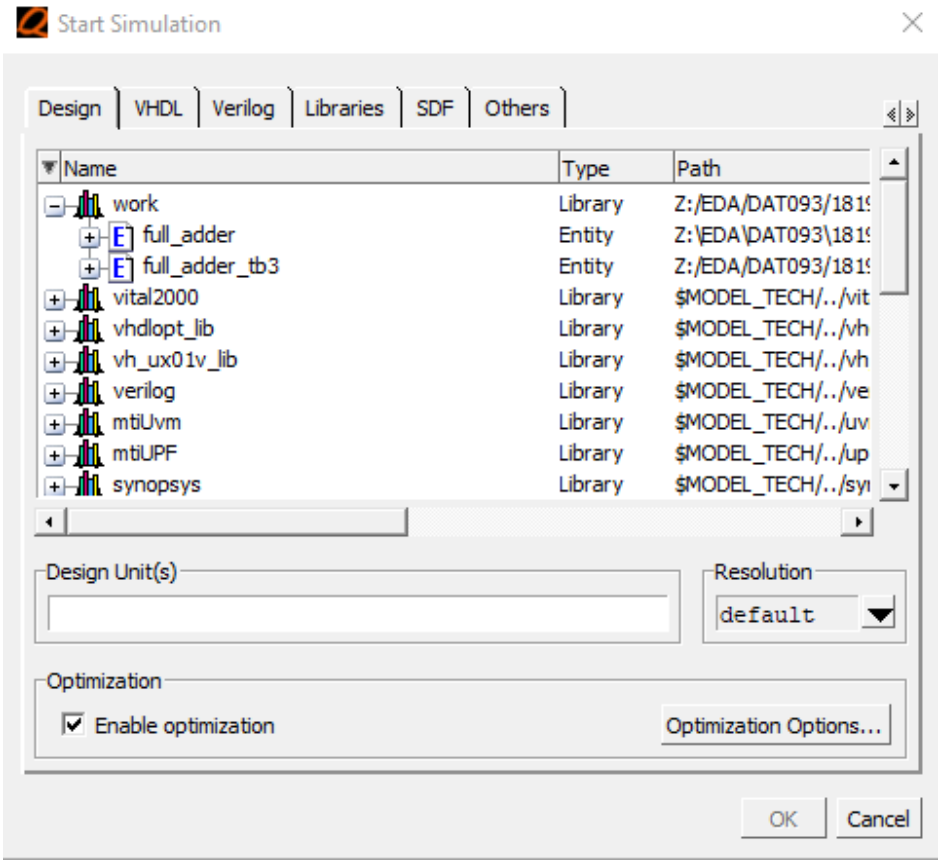
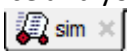


Figure 12 Select design to simulate

`full_adder_tb3`. The names you see in the work folder are the entities of the design, not the file names.

The main window will change appearance and you will see an Objects window with the signals in the design, *Figure 13* and a new tab 

has been added to the GUI.

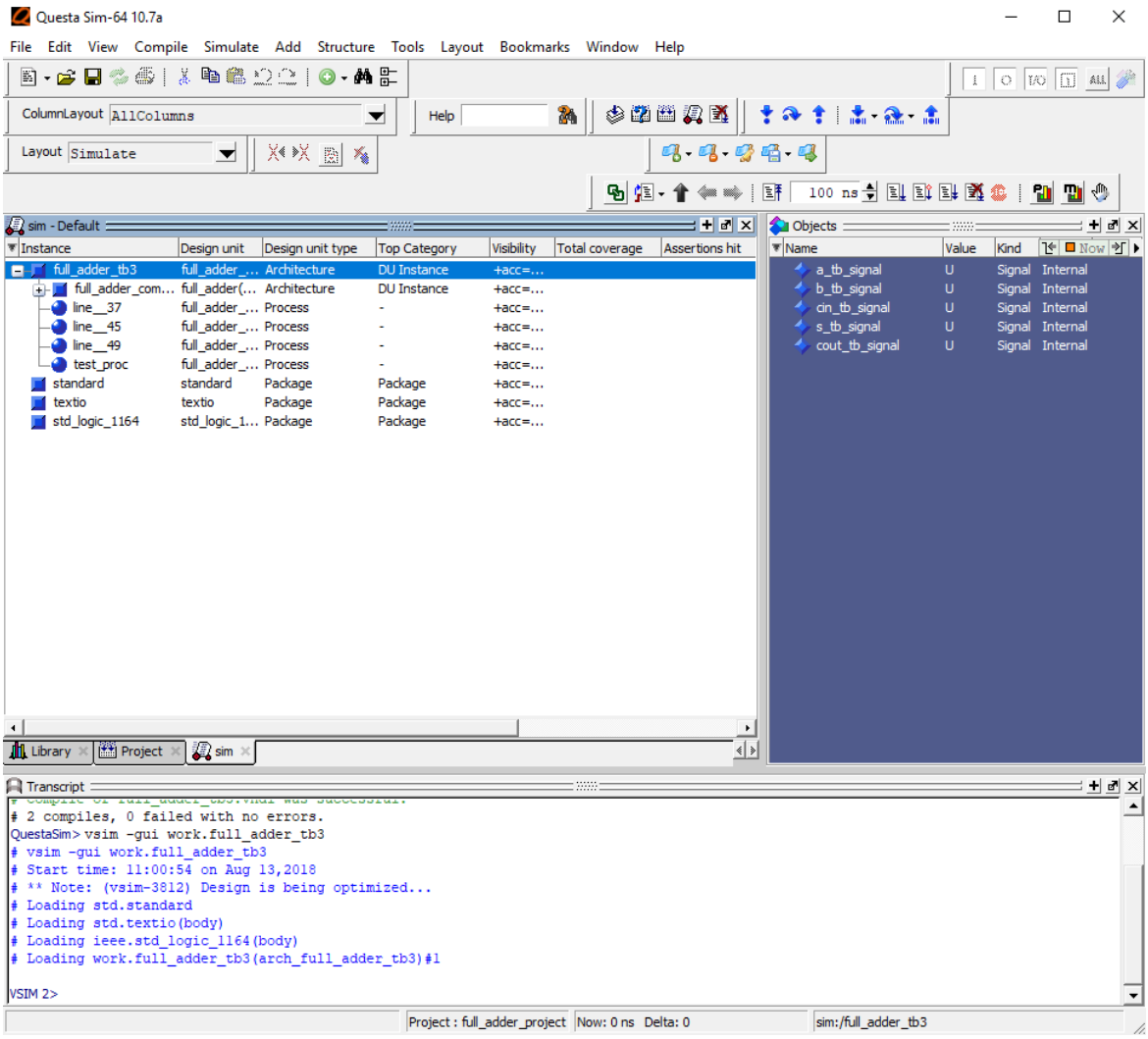


Figure 13 Simulation window

There is another way besides using the menus to start the simulation. You can select the 

tab, open the work folder, right click on the entity you want to simulate and select Simulate, *Figure 14*. There are some other simulation options in the Library tab, but we will leave them for now.

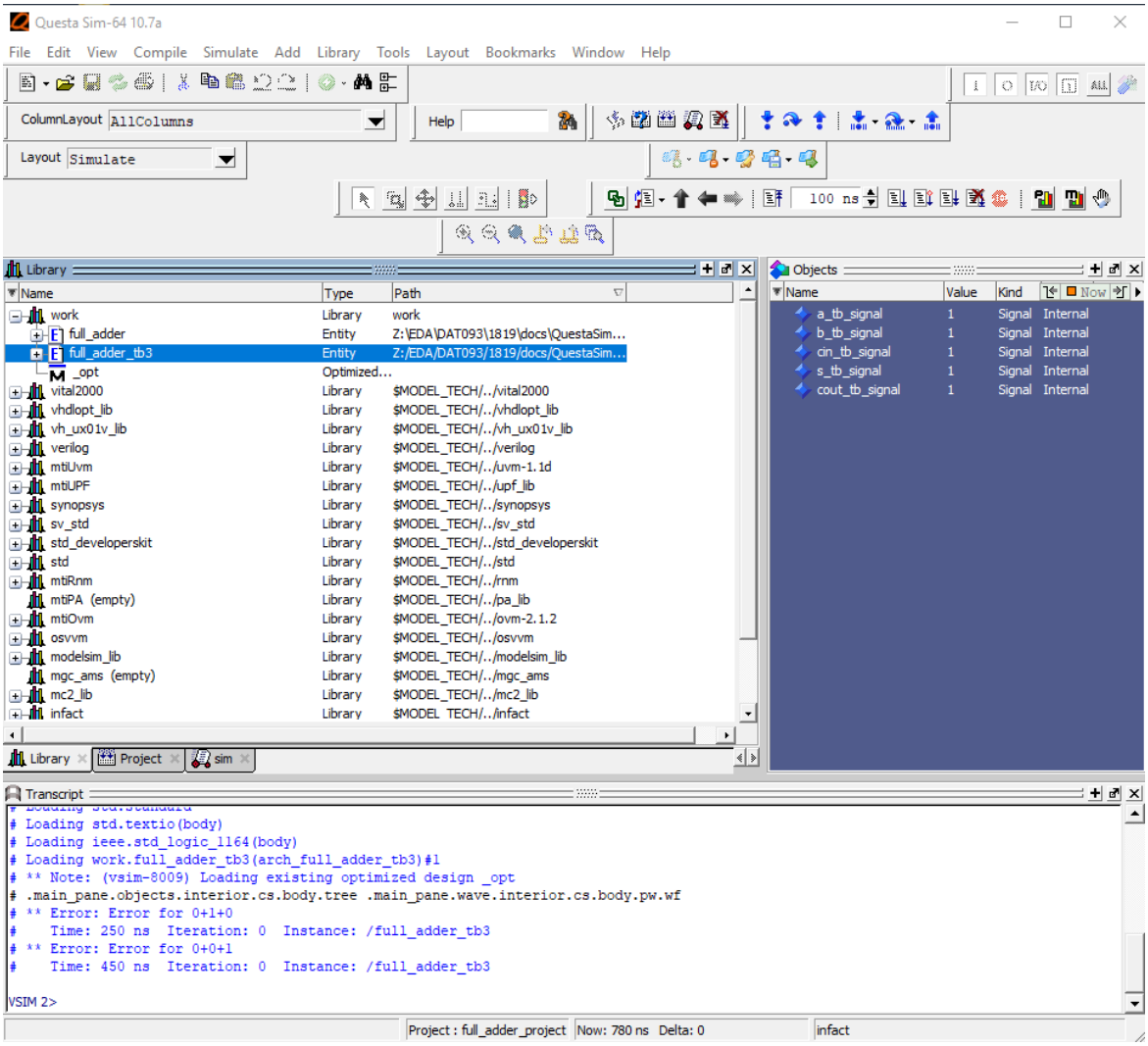


Figure 14 Simulating from the Library tab

To start and run the simulation script you type

```
do <name_of_do_file>.do
```

in the Transcript window, don´t forget the do ending, you won´t get that by default.

You can also start the simulation by right clicking on the do file in the Project tab and select Execute. If you type the do file name on the command line, then the do file will have to be placed in the project folder or you will have to add the search path to it when you type the command. If you right click on the do file in the Project tab to run it then it will run no matter where it is situated so that´s easier.

A new Wave window is added to the GUI, *Figure 15*, but now the GUi´s so crowded that it can´t really be used. You can turn any window of the GUI into a floating window by clicking on in the top right corner of the window and then you can drag the window to any size you like. In *Figure 16* we have done that with the Wave window.

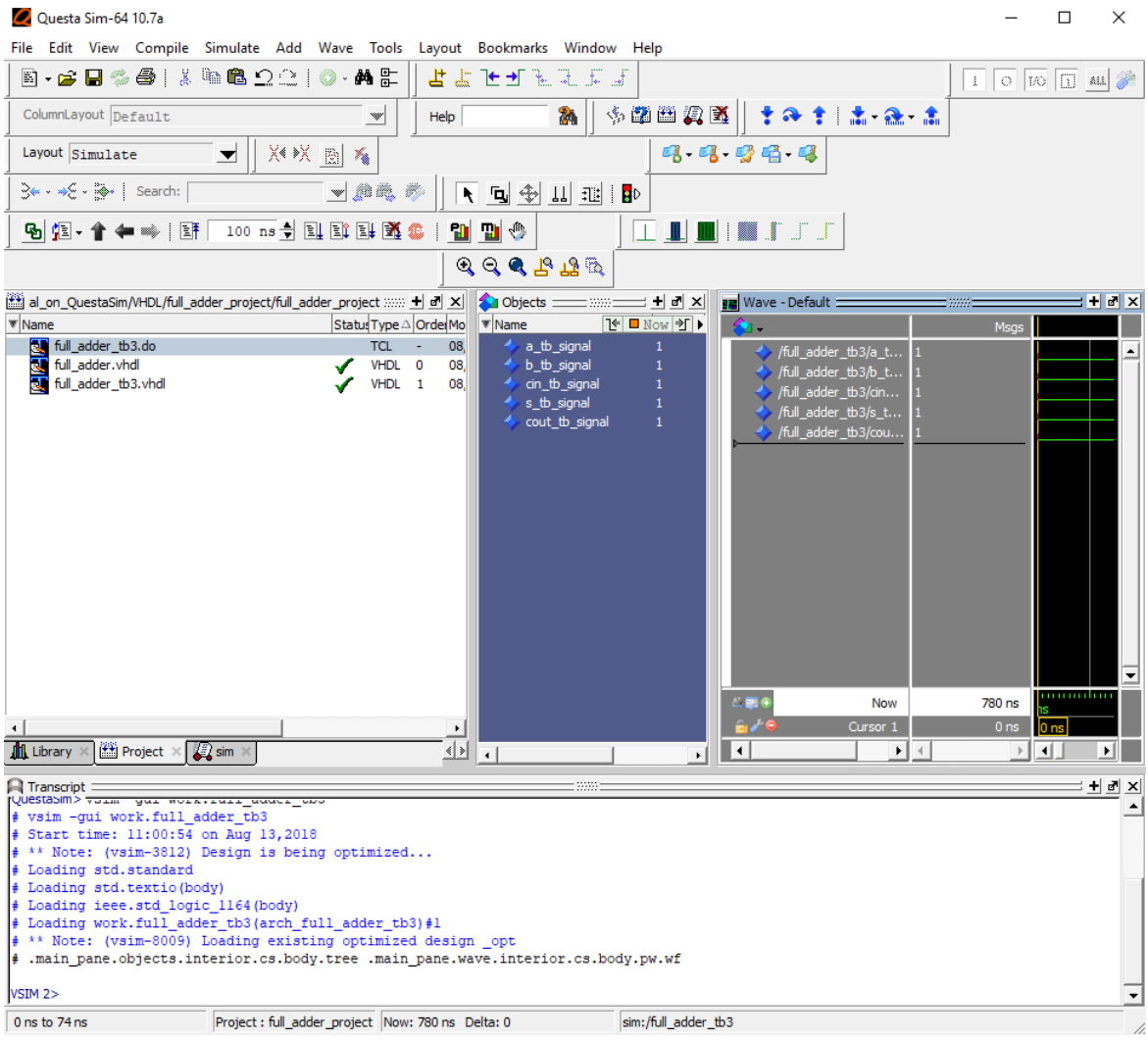


Figure 15 Simulation window

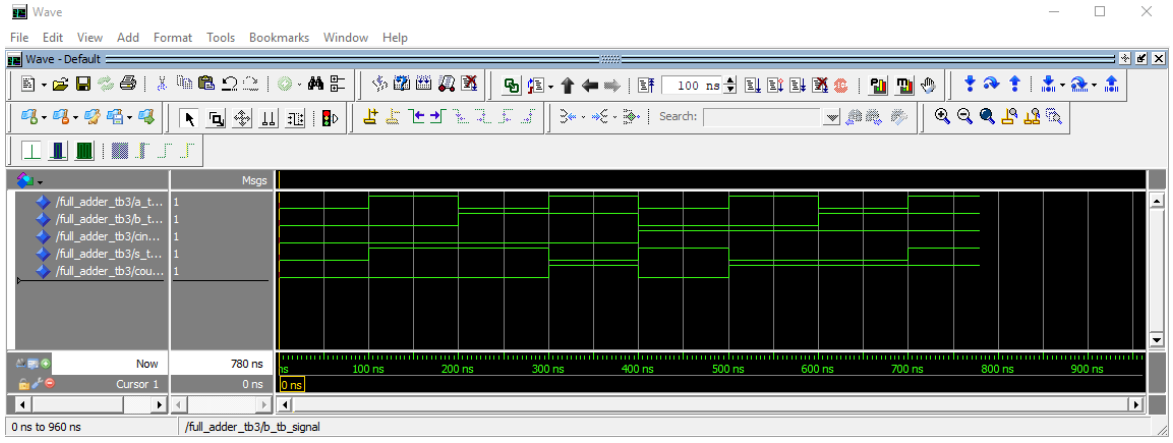


Figure 156 Waveform window

The Wave window will probably not look the way you want it to. Clean it up by changing the width of the columns and show the full simulation by right clicking on the actual waveforms and select Zoom Full, *Figure 17*.

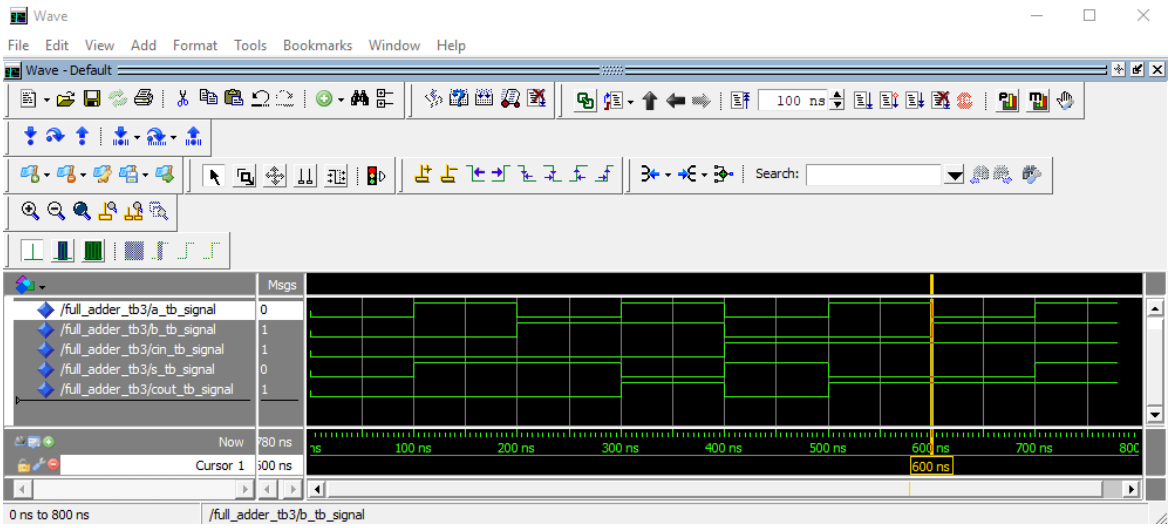


Figure 17 Cleaned waveform window

In the Msgs column you can see the signal values you have at the time where the yellow cursor line is placed. Click somewhere else in the waveform to see the values at that time.

If the simulation ran without errors, you will not get any error messages in the command window.

If the simulation gives errors these will show in the command window accompanied by an indication of the time when the error occurred, *Figure 17*. The error message doesn´t come automatically, it comes from what we have written in the test bench. You will not get any more indication of what caused the error so you will have to find that out on your own by studying the simulation result and the design files.

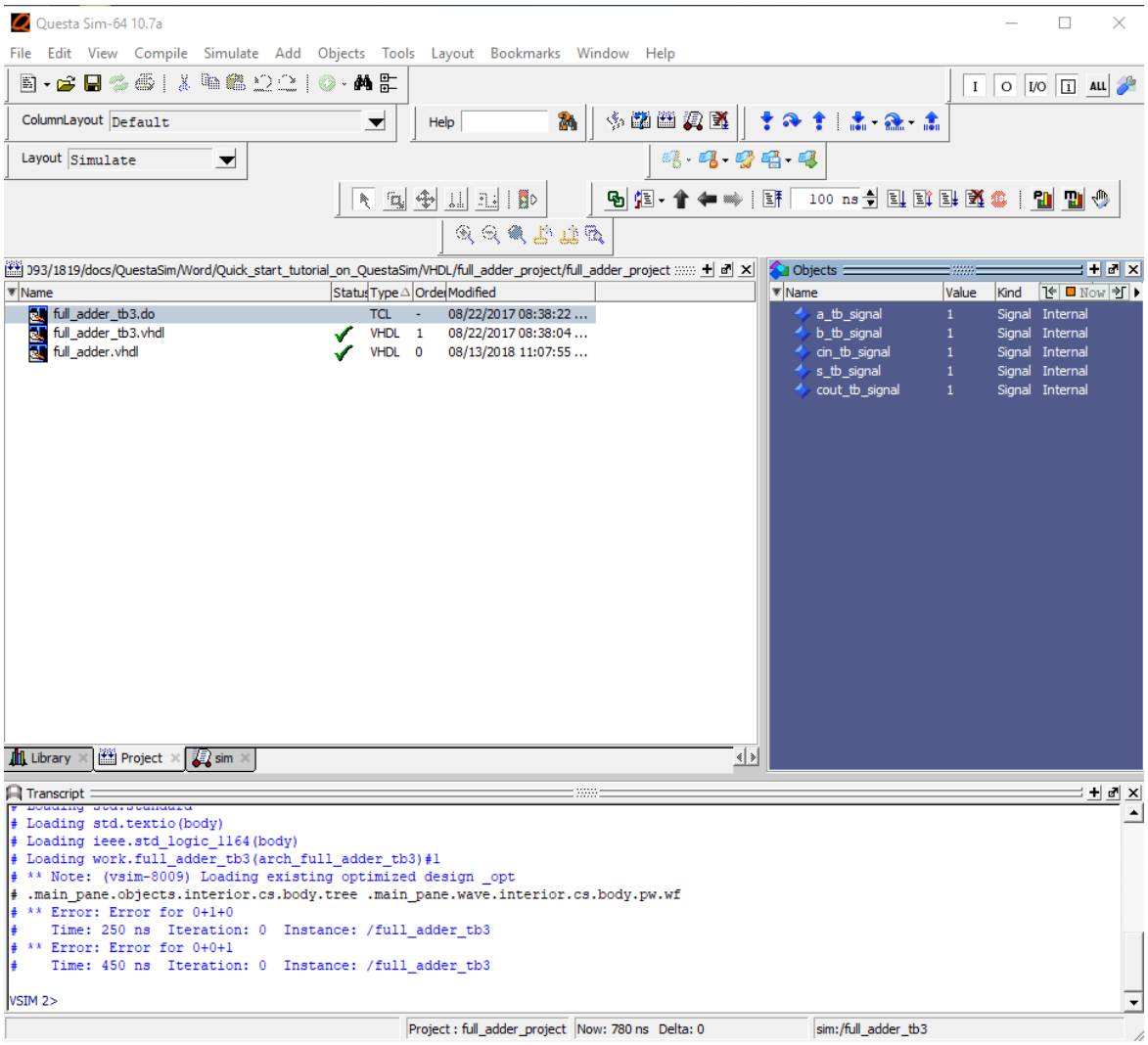


Figure 18 Simulation with errors

One error message that might appear when you start the simulation is a message saying that one or more of the components are unbound. This indicates that the entity of the component doesn´t match the component declaration and/or instantiation. If so change the entity of your design. Don´t do any changes in the test bench.

If the simulation gives errors or the results are incorrect then you must edit your VHDL files and recompile. After this you need to start a new simulation to read in the newly compiled file. You can close the old simulation before you do this but it is not necessary, you can just start a new simulation anyhow.