Administrivia

- Additional lab sessions are being scheduled
    - Monday mornings Oct 22 and 29
    - Show your results to get passed on each lab
- Digital exam: important info on PingPong

Power dissipation in electronic system design

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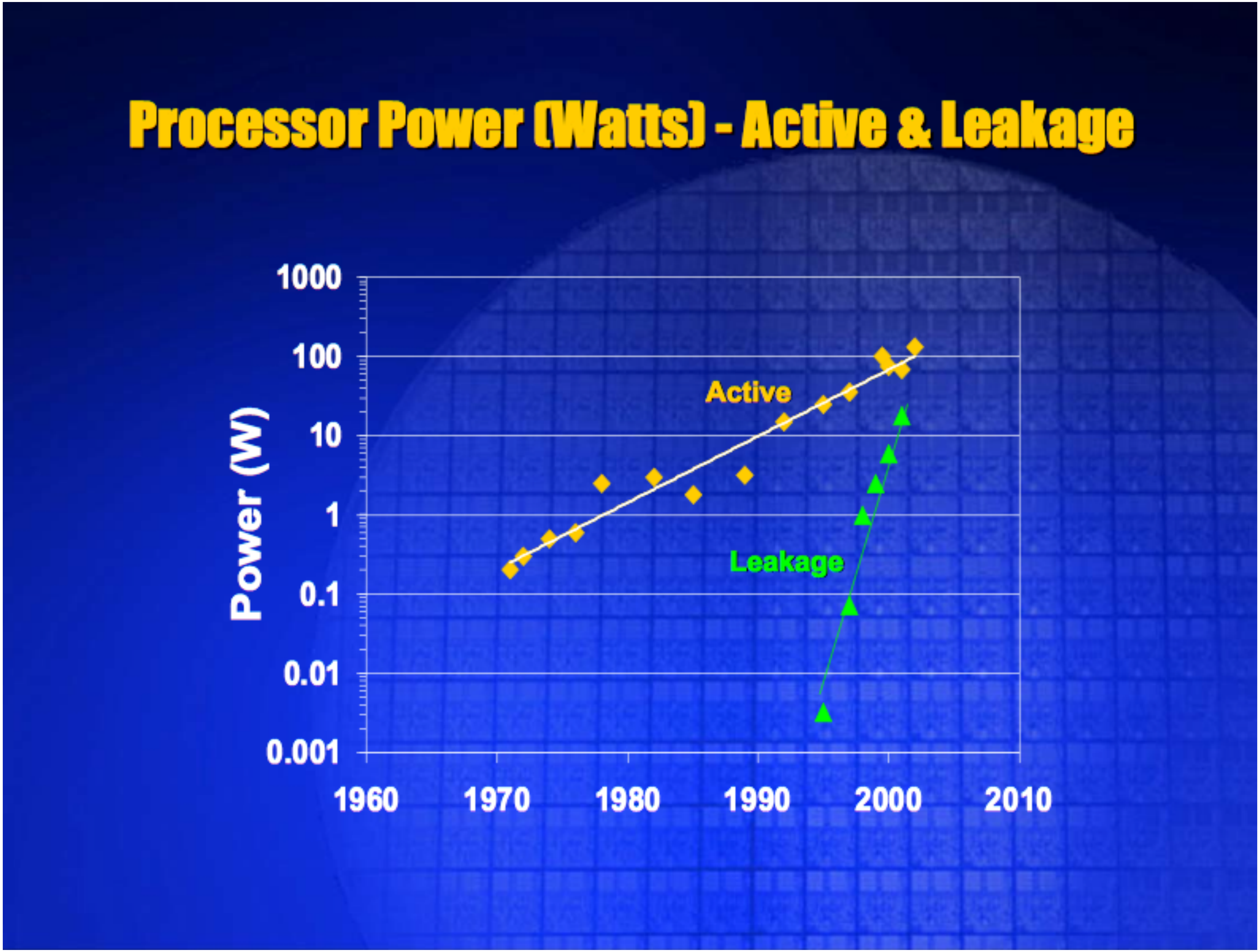
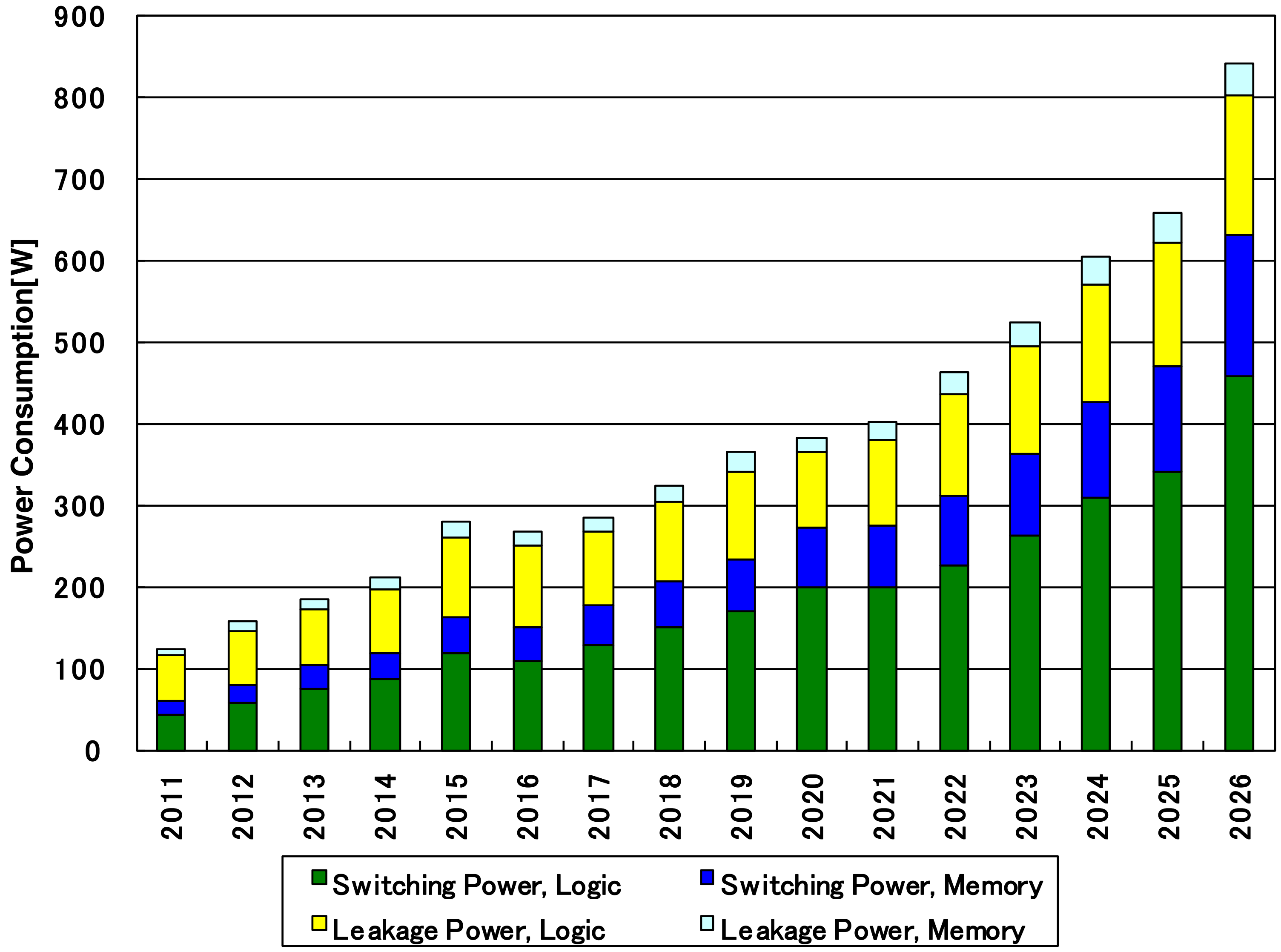
DAT093



Source: Intel

2011 processor-power predictions



- Drawing out 2011 trends of transistor, interconnect, etc
- Note: know how to cool ~150W from processor 😖
- Cooling clearly limits what can be done!

Hot topic for ~20 years

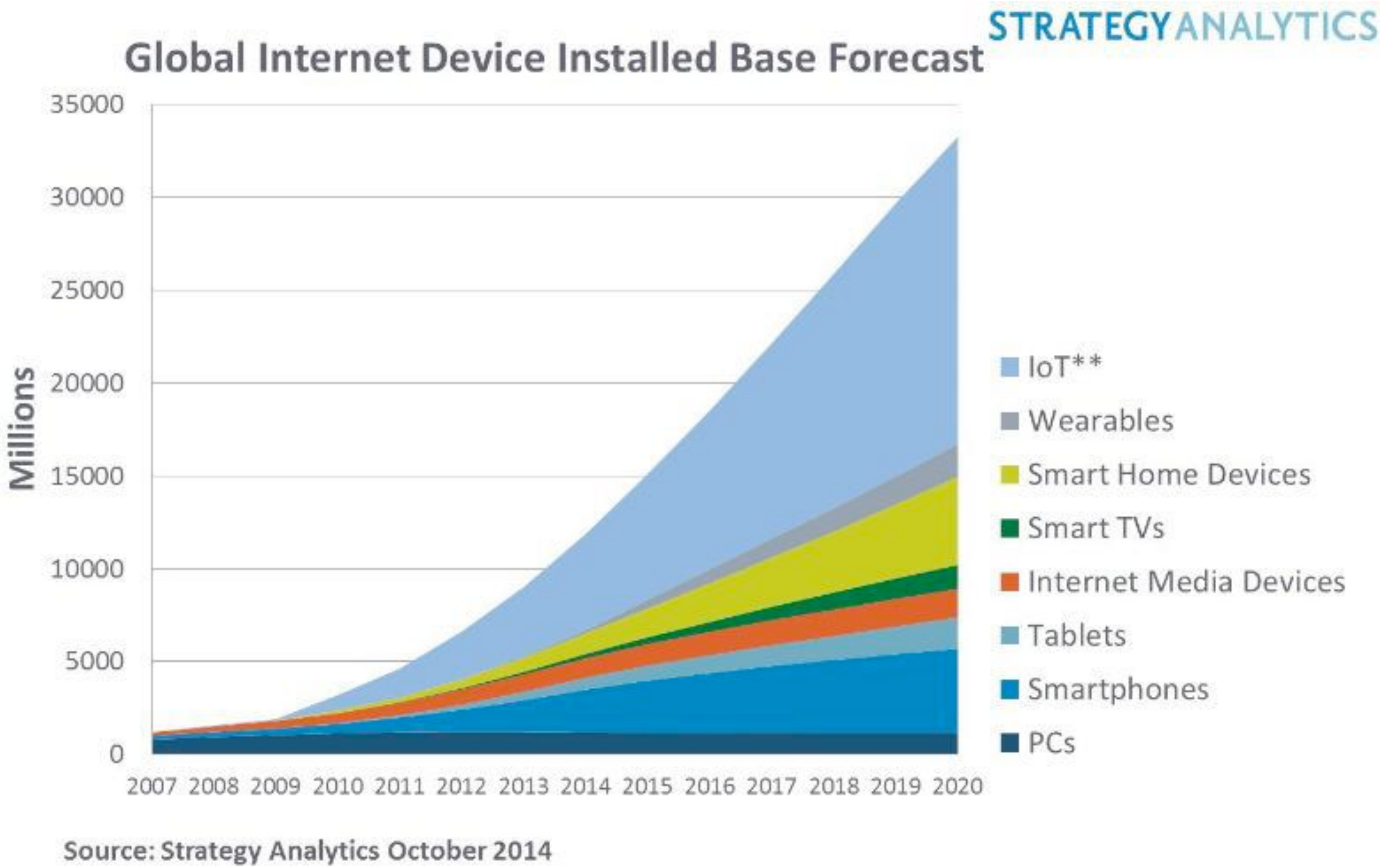
Why care?

- Batteries are heavy
  - Weight multiplies
- Power supplies are expensive
- Cooling is troublesome
  - Fans, heat sinks, heat pipes
- Hot circuitry has worse MTBF
- Power bill
- Environment

Perspectives

- Embedded
  - Autonomy, peak power
- Datacenters
  - Performance / W
- General purpose
  - Performance limit per package

Mobile computing



- Battery lifetime a major user requirement!

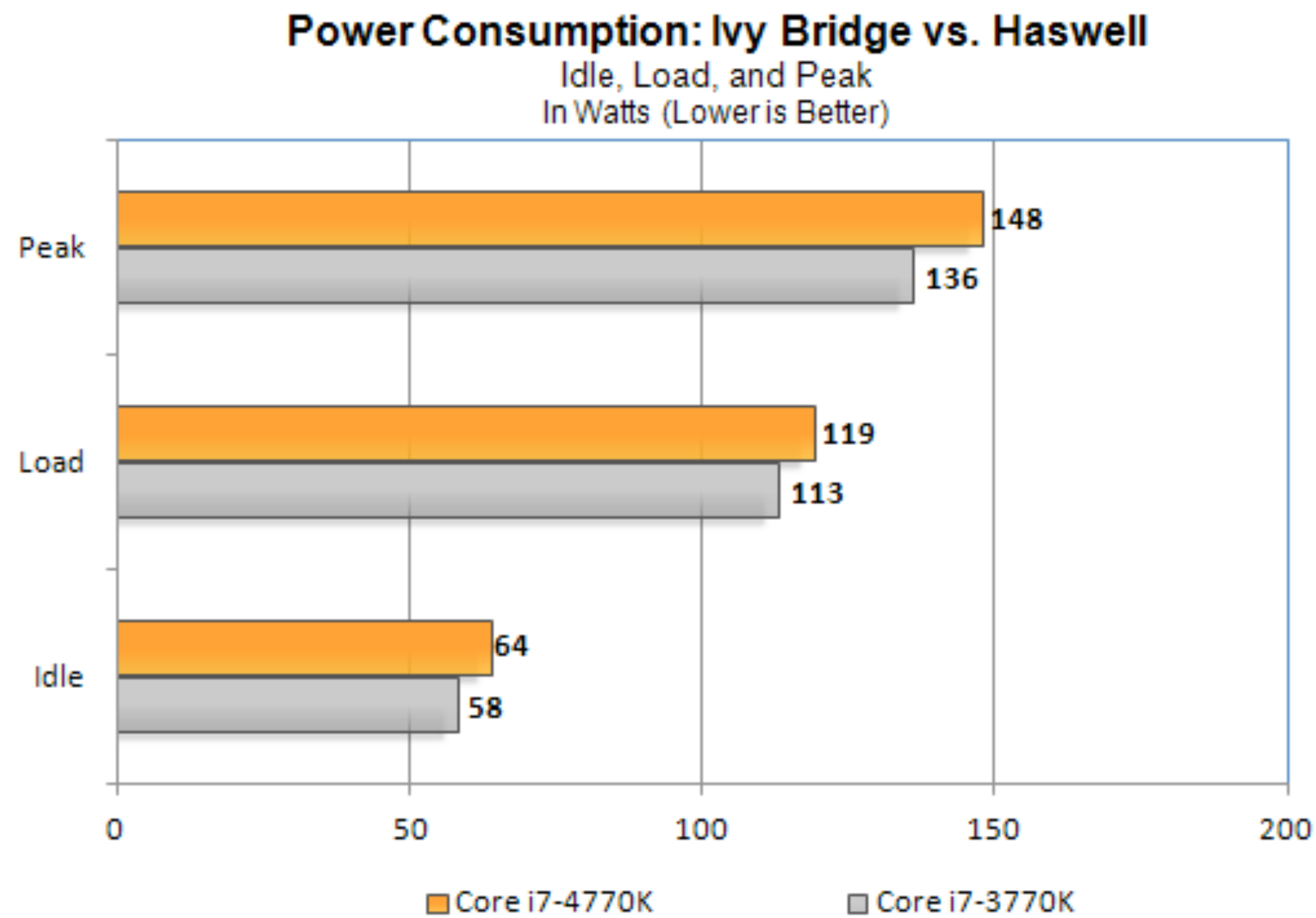
Why special focus lecture?

- Power traditionally “second class citizen” in design
  - Non-functional requirement
- More complex problem
  - Average case (power) vs worst case (delay)
- High-level simulations not straightforward
- Measurement and verification troublesome
  - Special equipment needed
  - Issues with accuracy, repeatability
  - Difficult to attribute to individual components

Two practical aspects

- Get power in
  - Provide circuits with high-quality supply voltages
- Get power out
  - Remove dissipated heat to keep circuits within reasonable operating temperatures
- Each more difficult at high power!

Power in



- 2012/2013 top-of-the-line Intel processors (Core i7)
- Note increase from idle to peak

[www.extremetech.com]

Power in

- High-performance server microprocessor:

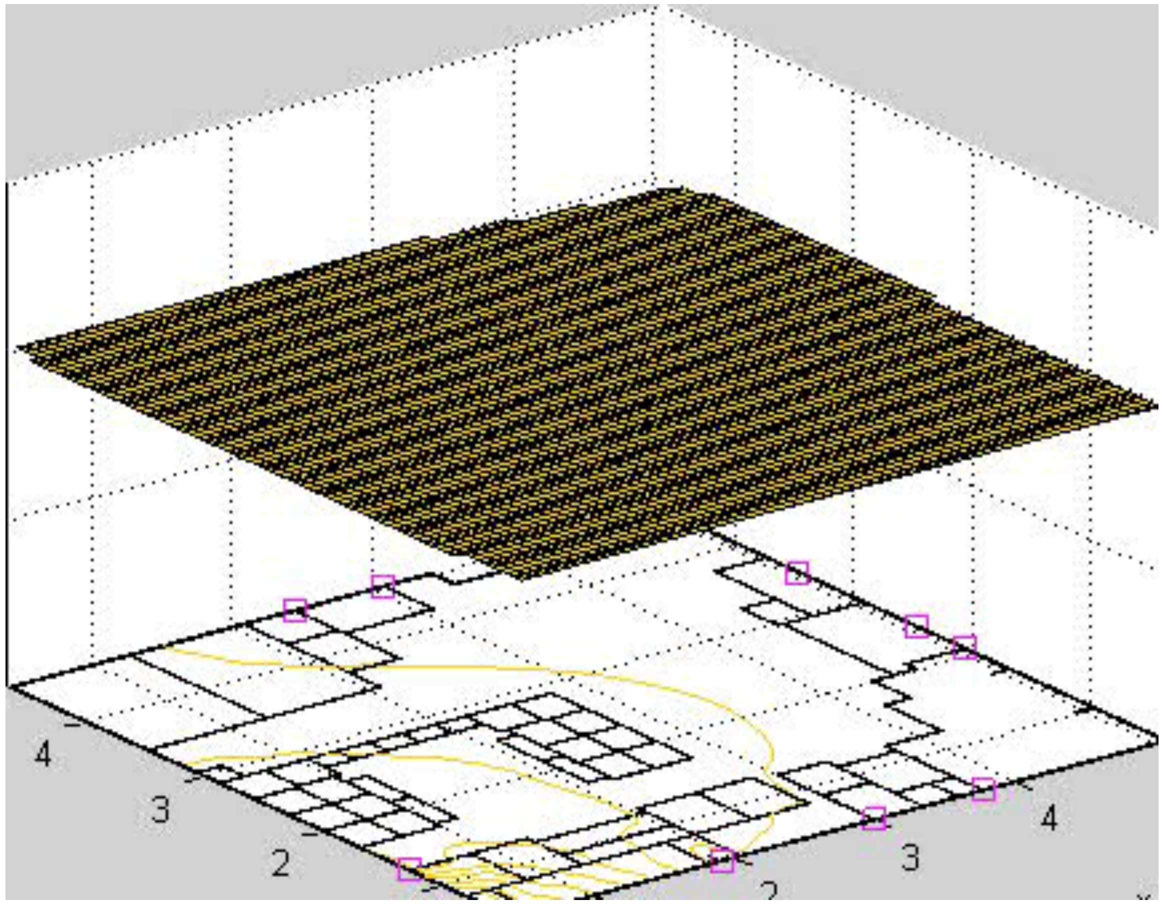
  148 W / 1 V = 148 A

[www.blocket.se]

Power in

- Quality as well as quantity!
- Most electronic circuits require well-controlled supply voltage
  - ± 10% typical spec. for digital circuits

On-chip voltage



- Small micro controller
  - 1 clock cycle
  - ~10% deviation from nominal V_{dd}

[Andersson et al, SPI'09]

Voltage regulators

- Maintain certain voltage regardless of current drawn
  - $I_{max} > 100 \cdot I_{min}$; high frequencies
- Voltage often settable / tunable
  - Dynamic Voltage Scaling (DVS)
- Specialized design problem
  - LC switching circuits, feedback theory

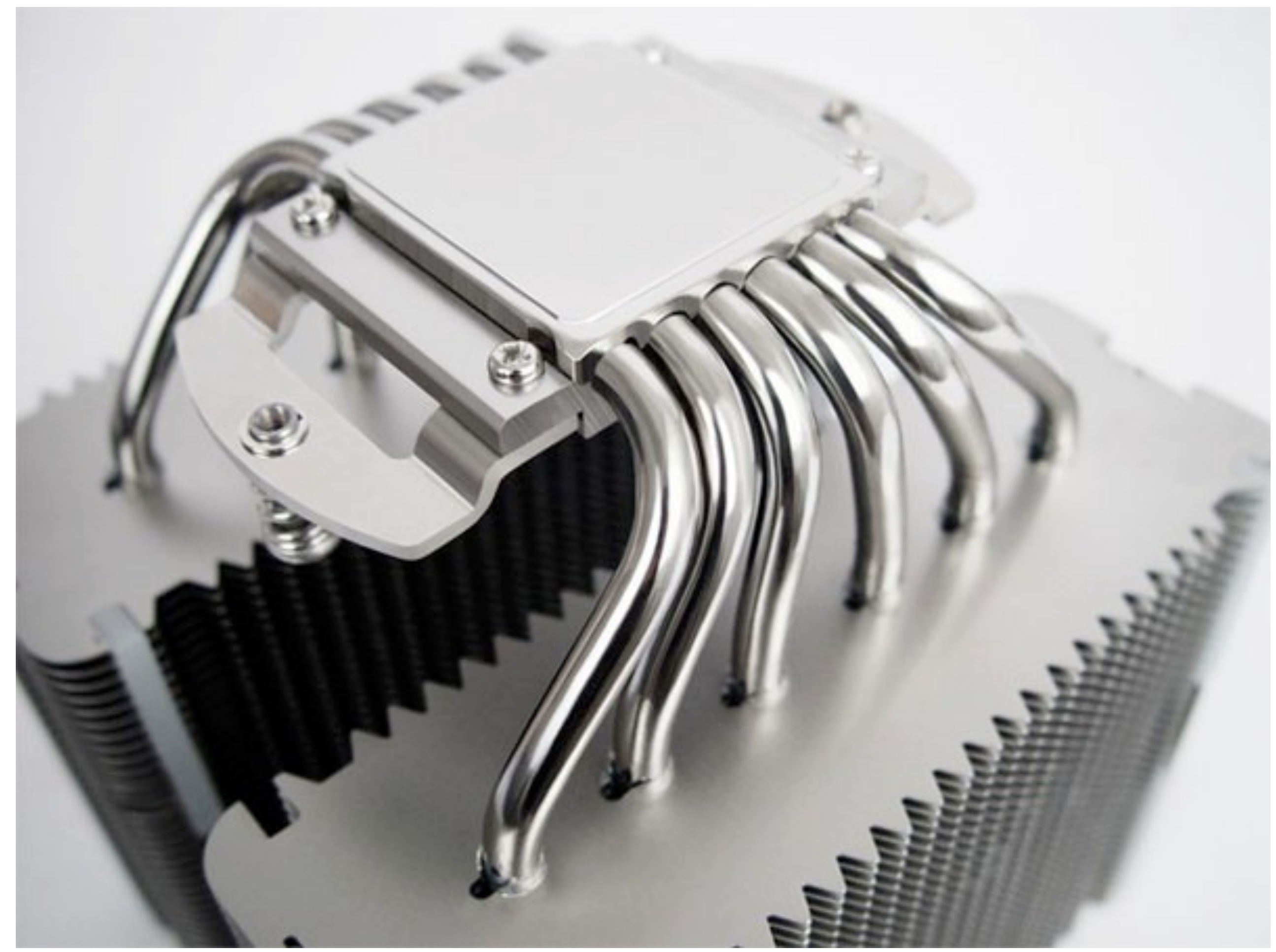
Power out

- Dissipated power heats circuits
  - Circuits cannot take high temps (typically 125°C)
  - Heat must be evacuated
- Compare:
  - Cooking hot plate: Ø = 20 cm, A = 314 cm^2, P = 2 kW: 7 W/cm^2
  - Microprocessor: A = 4 cm^2, P = 100 W: 25 W/cm^2
- How keep hot plate below 125°C?

Cooling

- Heat transport: conduction, convection, radiation
- Conduction: through package
  - Choice of material etc
- Convection: air / liquid flows past hot surface ("heat sink")
  - Thermal or forced w/ fans/pumps
    - Forced: expensive, noisy, failure-prone
- Radiation: sometimes only option (e.g. in space)

Heat sinks…



[www.dustin.se]

- 900 grams of metal

How reduce power requirements?

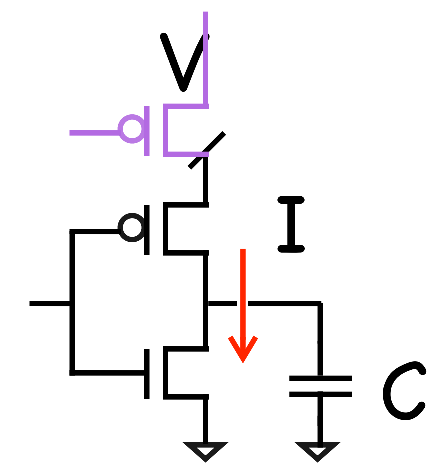
Background: Switching power

$$P = f \cdot C \cdot V^2$$

- Each transition means dissipation
  - Eliminate transitions (reduce f)
- Dissipation grows with C
  - Reduce C
- Dissipation grows (faster) with V
  - Reduce V …
  - …but only as far as performance allows
- Lower V_T allows lower V for same performance

Background: Idle power

- Current drawn even when not switching
- $I_{on} / I_{off} < 100$
- Worse for low V_T :-(
- Improve by supply cutoff
  - Best when gate, bulk voltages of cutoff device outside supply limits
  - Slow; energy cost per cutoff operation



Approaches / perspectives

1. Tech platform
2. Logic design
3. Clock gating
4. Supply voltage
5. Processors
6. Software
7. System arch
8. Project planning

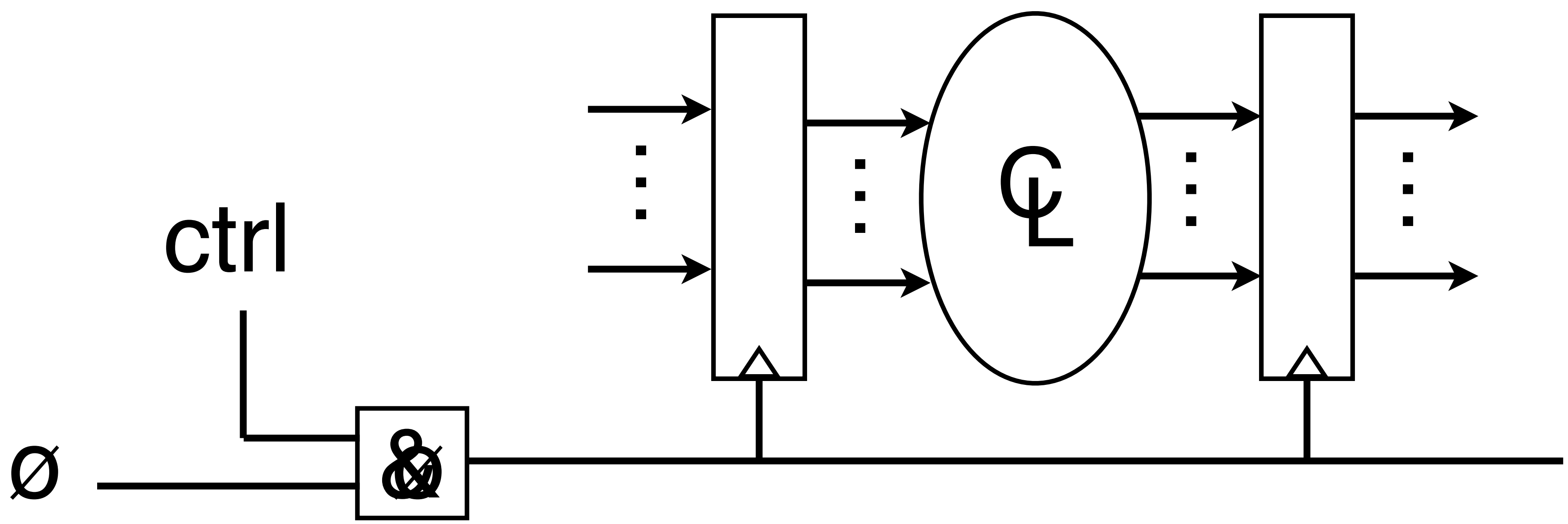
1. Implementation technology

- ASIC vs FPGA vs …
  - Typically at least 10x worse power for FPGA than for ASIC at same performance
  - Flexibility may make up for power deficit
- Later technology generations (“process nodes”) improve performance
  - Can be traded for power improvement
  - FPGAs get first dibs on new nodes
- Same operations in software may be much worse
  - IF, ID, EX, MEM, WB; plus cache misses, etc
- Trade power for flexibility

2. Logic-design level

- Logic-design style influences dissipation!
- Many ways to implement given logic function
  - Combinational
  - Sequential
- Low-power cell libraries
- Present synthesis tools do a good job here

3. Clock gating



- Switching in combinational logic when FFs change state
- Eliminate state change to reduce power
  - Also eliminate switching inside FFs
- Note: need to know that transformation is safe!
  - Tools may help with this (fine-grain)
- Also, need to ensure clock tree balancing (cf. MCC092)

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4. Supply voltage

- Power grows as V^2
  - Performance grows (more slowly) with V
- Select low but sufficient V
- Supply voltage often variable in modern designs
  - Ex: Microprocessors
  - V_{dd} typically under software control then
  - Verification issue!

MCC092

5. Processors

- Fetch, decode, execute, memory, writeback
  - Cache misses very expensive!
  - Major influence on power dissipation
- Embedded processors often designed for other optima than desktop processors
  - Compatibility, peak performance less important
  - Speculation means “useless work”
- Large power reduction possible when tailoring hardware to software

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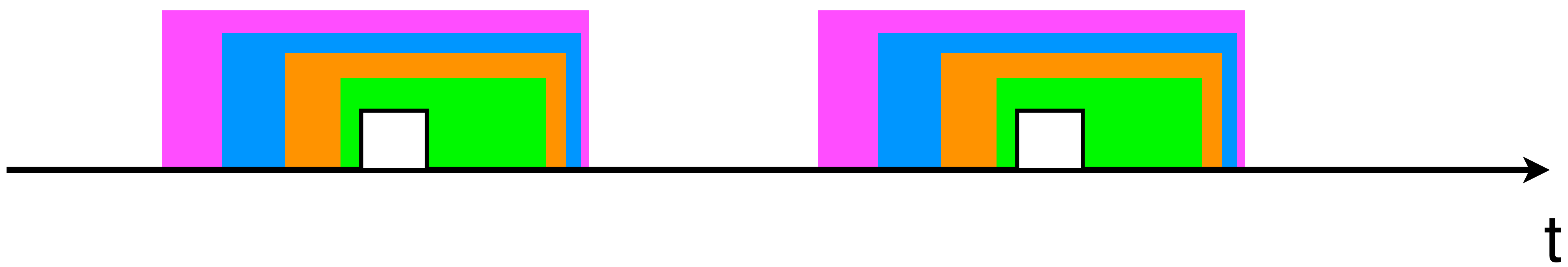
Processors, cont.

- Reduce power when performance not needed
  - Dynamic regulation of clock, voltage
  - Reconfiguration of memory systems
- Briefly exceed Thermal Design Power (TDP) limit using single core for v. high “peak” performance
  - “Turbo” mode (silly term, really)
  - Esp. useful for multicore processors

6. Software

- Software running on processor affects power (of course…)
- Carefully choose algorithms
    - Emphasize locality to avoid cache misses
- Modern processors offer hibernation
    - Software control

7. System level



- All design aspects must be coordinated
- Example:
  - Hibernation in frame-based wireless communication system
- Frame, processing, PLL, clock oscillator, supply

System example

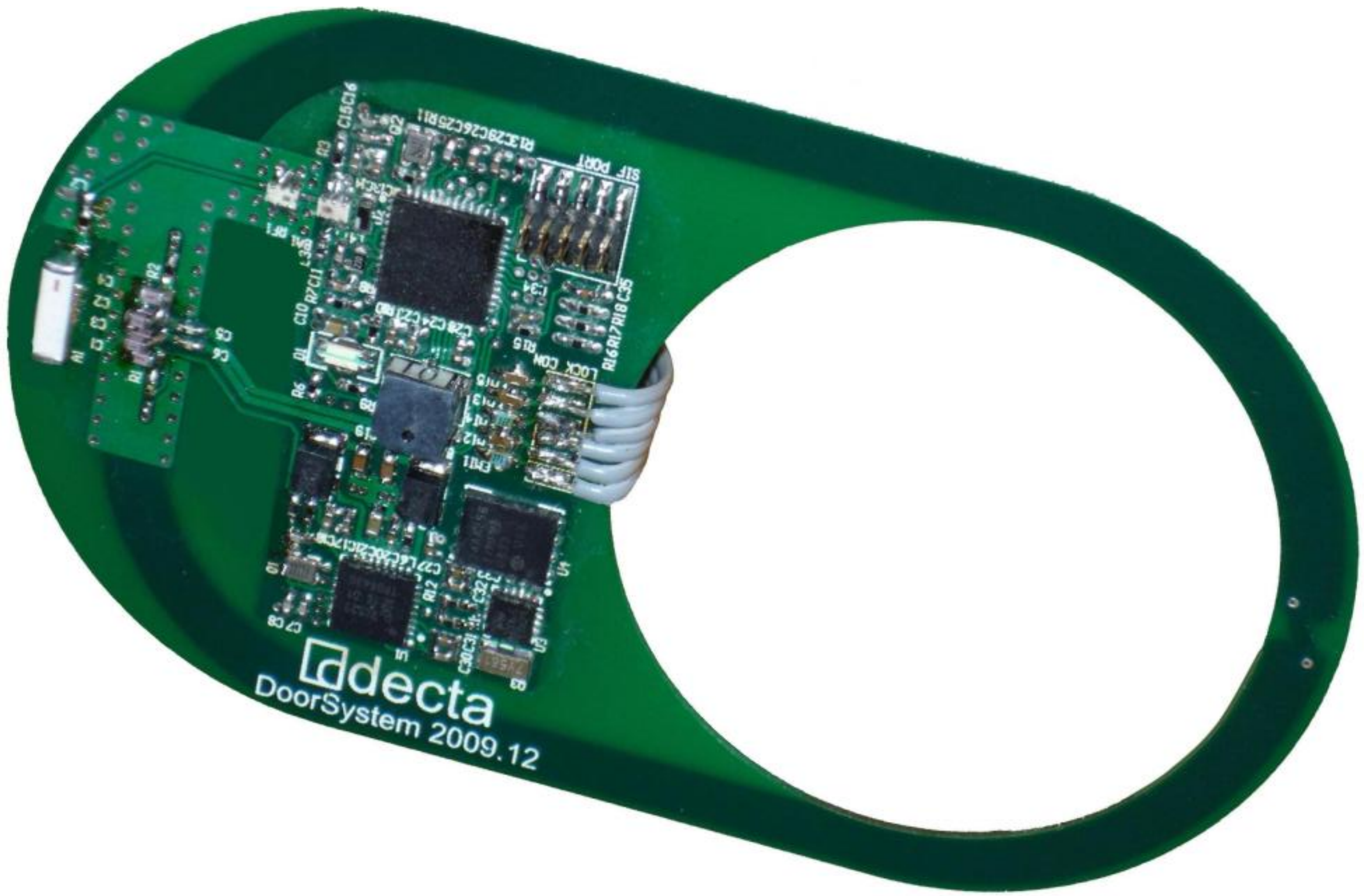
[Högrud, Riisberg-Jensen; thesis project in 2009-2010]

- Wireless door entry system
- Passive RFID card, wireless communication with database
- Fit <u>inside</u> door lock, incl. 2x AA batteries
  - 2-year battery life
  - Average current ≈ 142 uA

Example, cont.

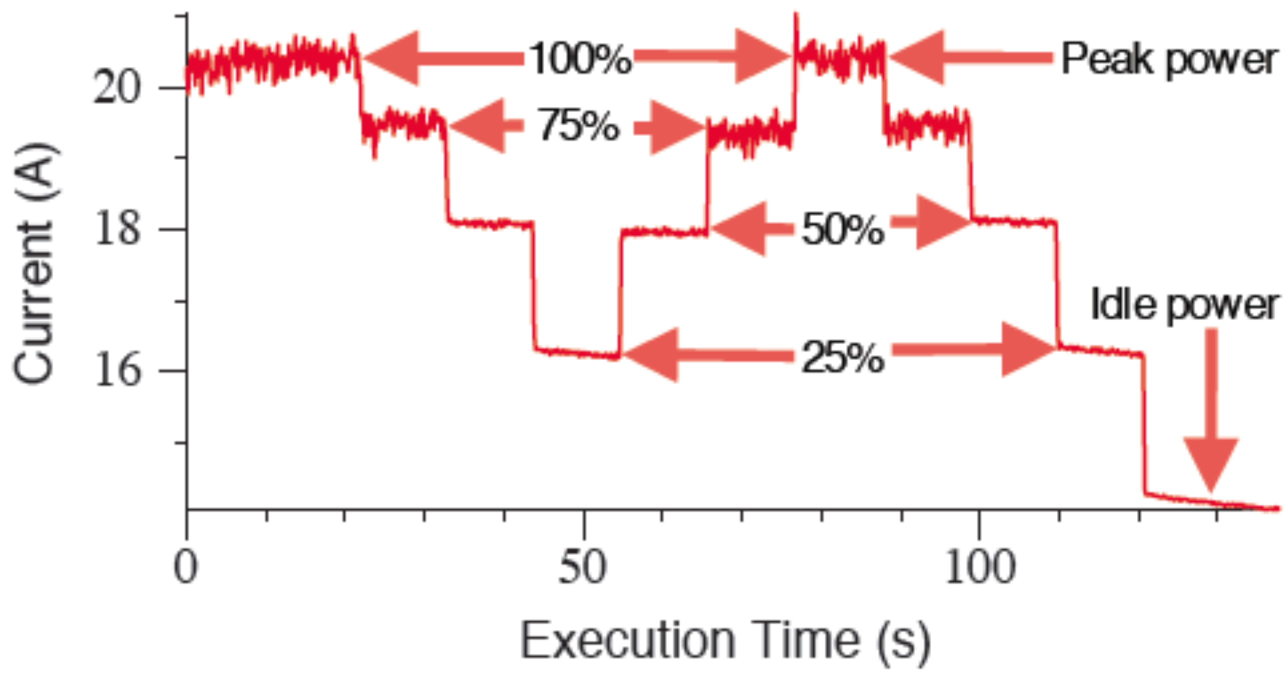
- Passive RFID uses polling
- Polling interval critical for user acceptance
- 1s deemed upper limit
  - Then, $I_{avg} \approx 960$ uA
- Added extra infrared proximity detector
  - Allows RFID circuits to stay idle

Production prototype



System example II

[Själander et al, MASCOTS '11]



- Cellphone base station baseband processing workload
  - Implemented on 64-core Tilera processor
- Key insight: advance knowledge of workload frame-by-frame
  - Move processors from/to idle state

8. Project planning level

- Power is a first-order concern in most design projects
  - Consider from day 1
- Tool-supported early prediction of power possible
  - Plan on using such tools

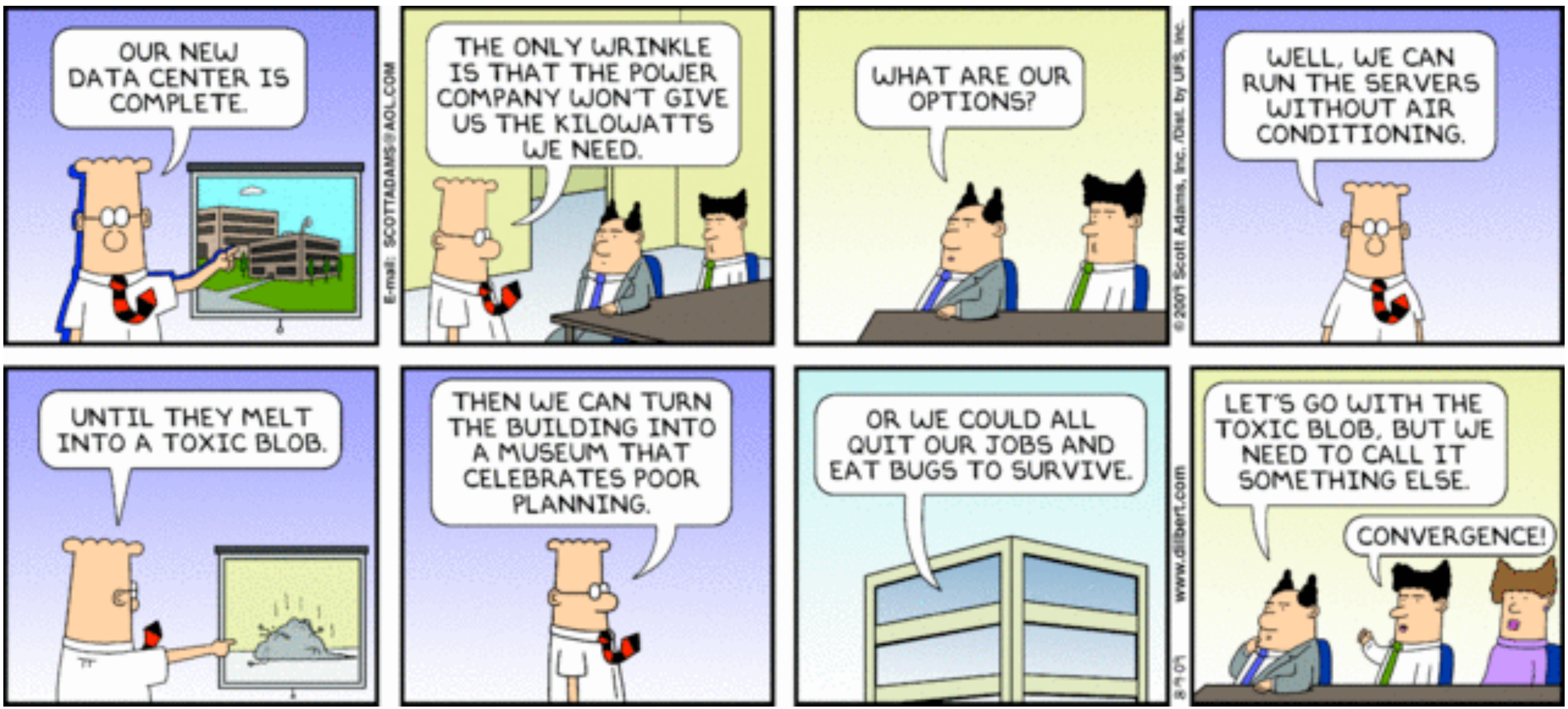
Summary

- Power dissipation issues pervade (almost) all modern electronic system design
  - Often most important parameter
- One bad design decision may neutralize many good ones
  - Consider from start, plan accordingly

Summary, cont.

- CAD tools are available for many power minimization tasks
  - Use them!
- Field still developing quickly
  - Follow the literature

Another perspective…



Is heat the problem?

- Not necessarily. But it <u>is</u> in the wrong place.
- Many of us actually use electricity to heat our houses!
- Might we look at the extra heat as a resource rather than a problem?

“Data furnace”

- Recent proposal by Liu et al (Microsoft Research)
  - Paper uploaded
- Split data center into suitable units (~100 CPUs)
- Rent these to home owners or other residential housing, for heating
- Link together with high-performance networks

Benefits

- Re-use energy, so reduce carbon footprint
- Computing close to people
  - Handy for information presentation
- Lower heating costs for consumers
  - …or they won't buy it :-)

Challenges

- Task distribution, resource usage
- Latencies challenge current cloud-computing models
- Information security
- Zero-touch management

Comments?

https://www.youtube.com/watch?v=IjeHKDh5I5g