A 400K-Transistor CMOS Sea-of-Gates Array with Continuous Track Allocation

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Abstract—A 0.8-μm CMOS sea-of-gates (SOG) array with first-level wiring channels perpendicular to transistor rows and 400K transistors is integrated on a 6×7-mm² chip. Implementation of a 64-bit multiplier shows 60-percent gate utilization and density of 1410 G/mm². The wiring length of the multiplier is 70 percent of that in a conventional SOG.

I. Introduction

THE COMPLEXITY of CMOS gate arrays has continued to increase as a key element for widespread applications. Recently, the sea-of-gates (SOG) array architecture, which employs carpeting gates in a core area of a chip, has become indispensable to implementing large-scale systems [1], [2]. The SOG has achieved almost 100-percent transistor utilization in an embedded RAM area. However, there remains the problem of low transistor utilization in the conventional SOG [3], because gate utilization is typically less than 35 percent in large-scale random-logic macrocell parts [1]. This paper discusses the problem and presents a new cell architecture to achieve higher gate complexity in CMOS SOG.

II. Cause of Low Transistor Utilization

A. Rough Track Allocation

The problem has been examined, and it is found that there are two factors which cause the waste of silicon in the logic parts.

The first factor in the waste of silicon is rough track allocation. Fig. 1 shows a layout scheme for our conventional SOG using the gate isolation technique [4], [5]. A basic cell (BC) is a pair of PMOS and NMOS transistors in the gate-isolated SOG. In this paper, row and column

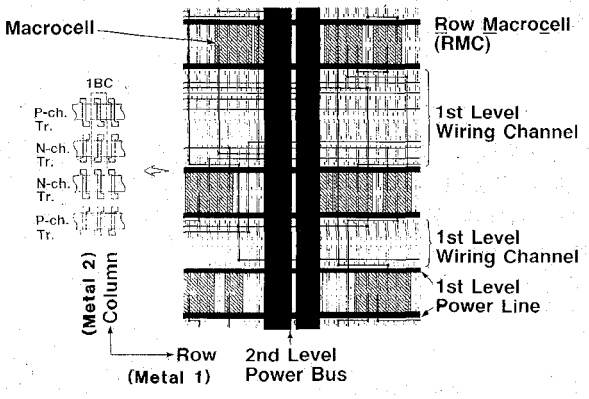

Fig. 1. Layout scheme of conventional gate-isolated SOG using RMC.

are defined as the directions along the gate length and the gate width, respectively. The BC's are carpeted in the core area of the SOG. The arrangement of the BC in the column direction is p-n-n-p channel type, which is effective in reducing the BC height for a given channel width of PMOS and NMOS transistors. The p-n-n-p arrangement has an advantage resulting from the sharing of power lines and well contacts between neighboring BC rows. Each macrocell, shown by oblique lines, is implemented by expanding cell boundaries along and within a BC row until enough gates are gathered for the macrocell. Thus, the cell architecture is named row macrocell (RMC). The first-level wiring runs along the BC row and on the first-level wiring channel which is varied by one BC row pitch in this structure. Fig. 2 shows an example of a wiring track distribution in a logic system laid out by using the RMC structure. The horizontal axis indicates each assigned wiring channel number in the logic system, and the vertical axis indicates the track counts in each channel. The broken line shows the track counts actually required for the layout of the logic system, while the solid line shows the actual track counts allocated by our layout system. The allocated tracks are adjusted coarsely because the variation in the channel allocation is one BC row which corresponds to 15 tracks in this case. Consequently, most of allocated tracks happen to remain unused. In the worst case, one BC row is allocated for only a one-track shortage. This is the main reason of

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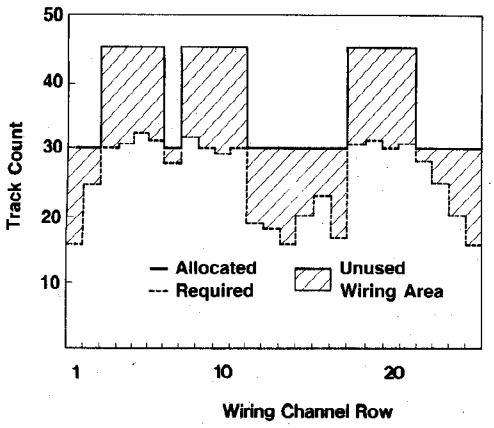


Fig. 2. Track distribution in SOG using RMC: allocated tracks versus required tracks.

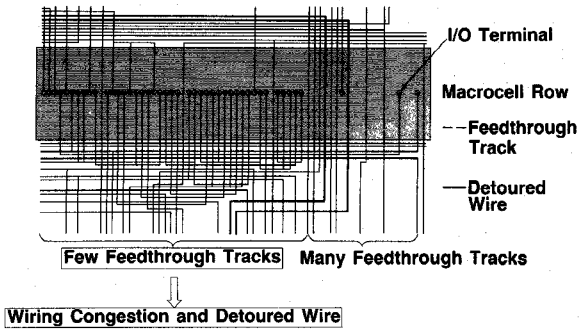


Fig. 3. Part of RMC layout showing wiring congestion.

the low transistor utilization in the logic parts. In other words, minimization of track increment is the key to increasing gate utilization.

B. Wiring Congestion in Conventional SOG

Fig. 3 illustrates a part of layout pattern in the conventional RMC structure. There are many feedthrough tracks on the right side. On the other hand, macrocell regions with very few feedthrough tracks frequently appear as shown on the left side, where primitive gates are placed closely. This is because the primitive gates such as NAND gates and NOR gates have no feedthrough track per macrocell (see Section III-C). In the wiring area adjacent to a region with few feedthrough tracks, local wiring congestion can occur. Moreover, when feedthrough wiring is blocked, some wires have to be detoured as indicated by bold lines. Therefore, preparing sufficient feedthrough tracks even in the primitive gates is essential to improve routability and to minimize the depopulated gates for feedthrough tracks.

Some articles report that fine track adjustment is achieved by reducing the BC height [6]. This approach, however, results in incomplete intra-cell wiring of macrocell libraries. Employing an extra layer metallization is reported to improve the gate utilization due to the increase of wiring area [7], but this approach results in a longer turnaround time and lower fabrication yield because of extra process steps [8].

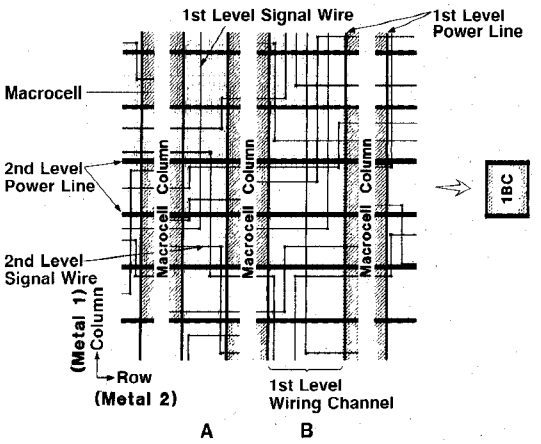


Fig. 4. Layout scheme of SOG using CMC.

To overcome these problems, a new cell architecture named column macrocell (CMC) is proposed.

III. Column Macrocell

A. Layout Scheme (Continuous Track Allocation)

Fig. 4 shows a layout scheme of the CMC. Macrocells in the CMC structure are indicated by oblique lines. The BC of the CMC is defined as shown on the right side. The concept of the CMC is to implement any macrocell by stacking the BC's along the column direction until enough gates are accumulated for the macrocells. The second-level power lines are shared by every two adjacent BC rows. In the CMC structure, the first-level wiring runs along the poly-Si gate of transistors in the column direction. Therefore, the width of the first-level wiring channels is able to be incremented by one column of p-channel and n-channel transistor chains. For example, the channel *A* corresponds to a width of four columns, and the channel *B* has a width of seven columns. In other words, the track increment of the CMC is only one, which is the ideal value for track allocation. Consequently, only as many tracks as required in each channel are assigned in the SOG employing the CMC. This continuous track allocation is the key feature of the CMC.

B. BC Design

The macrocells of the CMC, except big cells such as RAM, are basically a poly-cell structure as described in Section III-A. Therefore, the number of p- and n-channel pair transistors (N_{pn}) in one basic cell including isolation transistor pairs was carefully determined after considering the trade-off between the feasibility of 130 different kinds of macrocell layout and the total macrocell area for implementing logic systems. Fig. 5 shows the total macrocell area (A_{tm}) required for implementing logic systems and the number of layout-incomplete macrocells (N_{um}) as a function of N_{pn}. Logic system *A* consists of a large percentage of primitive gates, while logic system *B* consists of a large percentage of complex gates such as flip-flops.

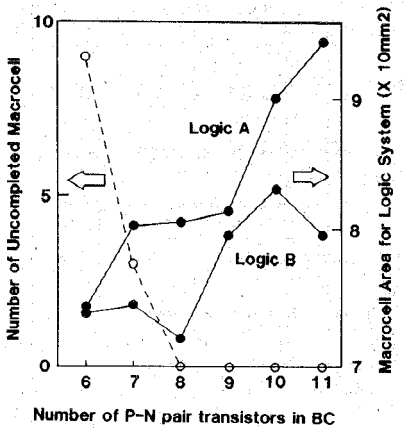


Fig. 5. Total macrocell area required for logic systems versus number of p- and n-channel pair transistors in the BC.

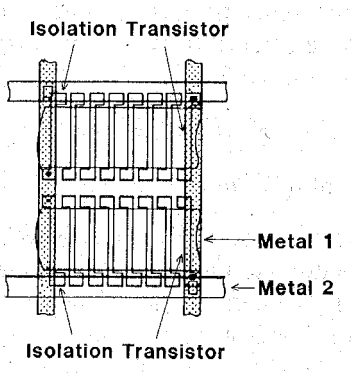


Fig. 6. Basic cell of CMC.

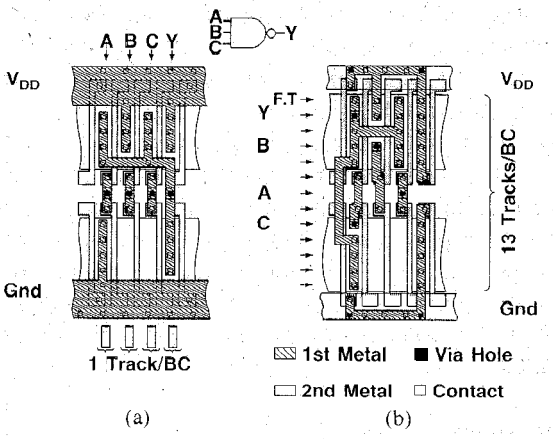


Fig. 7. Example of macrocell layout (three-input NAND): (a) RMC and (b) CMC.

Intracell wiring of all column macrocells is performed using only first-level metals and poly-Si gates. Since the width of a BC with N_{pn} of less than 8 is narrow for intracell wiring, there are layout-incomplete macrocells. When N_{pn} is 8 or greater, A_{tm} increases as N_{pn} increases. Consequently, N_{pn} has been determined to be 8. Fig. 6 shows the BC's of the CMC. First-level power lines run along the isolating transistors on both sides of the BC's, while second-level power lines are shared by adjacent BC's. All macrocells of the CMC are implemented by stacking BC's.

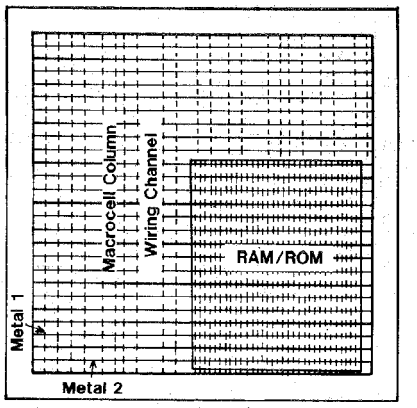


Fig. 8. Chip image of CMC.

C. Macrocell Layout (Sufficient Feedthrough Tracks)

CMC also has the advantage of having sufficient feedthrough tracks per macrocell for the routing process. Fig. 7 compares the cell layouts of the RMC and CMC for a three-input NAND primitive gate. Fig. 7(a) shows the layout pattern on the RMC structure. There is only one feedthrough track per BC in the RMC, and all the tracks are used for I/O terminals.

On the other hand, the CMC reserves 13 feedthrough tracks per BC as shown in Fig. 7(b). The cell layout of any column macrocell is performed using only first-level metals except for power lines. So, there remain nine feedthrough tracks in this gate. In any other multiple-input gates or more complicated gates using CMC, there exist sufficient feedthrough tracks for routing. This feature results in the reduction of detoured wires and net wiring length.

D. Chip Image of SOG using CMC (Fine Mesh Power Distribution)

Since the gate-isolated RMC does not have the capability of mesh power distribution per macrocell due to its variable-width structure and insufficient feedthrough tracks, a few wide power buses using second-level metals are used for power distribution as shown in Fig. 1. Location and size of big cells such as large macrocells and memories are restricted between the power buses.

On the other hand, CMC provides a fine mesh power distribution. Fig. 8 illustrates a chip image of a SOG using CMC. The core area is constructed by carpeting BC's of the gate isolation structure. Since the CMC structure has sufficient feedthrough tracks per BC, the fine mesh power distribution per row and column of BC is available. This power distribution scheme makes it possible to place macrocells of any size anywhere on the CMC structure.

IV. Comparison of Layout Results

A. Layout Experiment

To compare the gate densities on the chip level using the CMC and RMC approaches, layout experiments have been

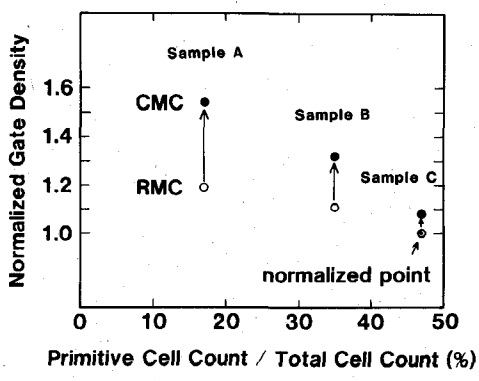


Fig. 9. Gate densities of the CMC and RMC approaches for random logic systems as a function of primitive cell percentage.

performed based on the two types of BC's. The CMC BC consists of eight transistor pairs as described in Section III-B, while the RMC BC consists of one transistor pair. P- and n-channel pair transistors in the two types of BC's are defined as equal in both directions along the gate length and the gate width. Wiring pitch is set equal in the CMC and RMC.

Since the CMC does not require special layout tools, all layouts are completed using an in-house layout system which has been used for the conventional RMC structure [5]. The layout is as follows:

1) placement is performed using the min-cut method so that cut lines are set to give priority to second-level wiring;
2) prior to routing, in-house program "CHANTA" counts the required tracks in each wiring channel and decides automatically how many columns or rows of p- and n-channel transistor chains have to be used as wiring channels in the CMC and RMC cases, respectively;
3) loose routing and detailed routing based on a channel router are performed.

B. Layout Results

Although the CMC structure has advantages in layout over the gate-isolated RMC, unused transistors are unavoidable the same as in the usual oxide-isolated BC structures, especially in primitive macrocells such as NAND gates. Thus, three types of random logic systems, which are classified by the percentage of primitive macrocells, have been chosen for the layout experiment using CMC and RMC.

Fig. 9 shows the gate density in three types of logic systems. The gate counts of samples *A*, *B*, and *C* are 28.5K, 18.5K, and 17K gates, respectively. The horizontal axis indicates primitive macrocell percentage. In the comparison, the primitive macrocell means inverter, two-input AND, two-input NAND, or two-input NOR, and the total cell count means the number of macrocells utilized in each circuit. The gate density is normalized by the value of the RMC to 47-percent primitive macrocells, which is the largest percentage in the circuits that we have ever implemented on SOG. CMC achieves 1.08 to 1.31 times higher gate density than that of RMC.

TABLE I
COMPARISON OF LAYOUT RESULTS OF CMC AND RMC

	Sample A		Sample B		Sample C	
	RMC	CMC	RMC	CMC	RMC	CMC
Core Area Size(mm^2)	36.8	29.5	26.3	23.1	27.2	25.3
Macrocell Area (%)	48.3	57.5	37.3	48.6	32.6	45.5
Wiring Area (%)	51.7	42.5	62.7	51.4	67.4	54.5
Used Feedthrough Count	33715	35030	15266	29040	14000	35085
Average Wiring Length (mm)	0.68	0.43	0.91	1.05	0.88	0.84
(1st Level)	0.23	0.20	0.42	0.44	0.45	0.35
(2nd Level)	0.45	0.23	0.49	0.61	0.43	0.49
Primitive Macrocell (%)	17		35		47	

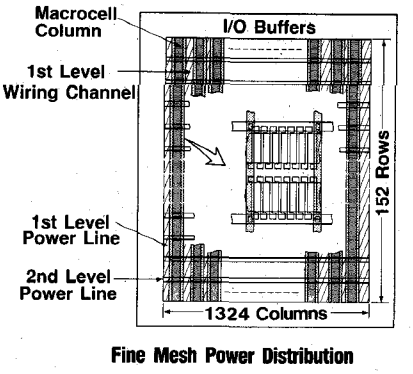


Fig. 10. Configuration of SOG employing CMC.

Table I summarizes the layout characteristics. The macrocell areas and the wiring areas are shown with percentages to the core area size. The wiring areas of the CMC are 60 to 75 percent of those of the RMC because of increases in the used feedthrough tracks. The macrocell area of the CMC grows larger than that of the RMC as the primitive macrocell percentage increases. Consequently, the advantage of CMC over RMC decreases with the increased primitive macrocell percentage. These results, however, indicate that the CMC approach achieves a higher gate density than the conventional RMC approach in most types of logic systems.

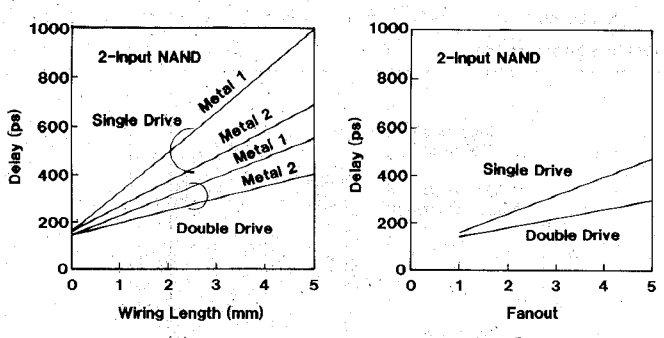
V. CHIP DESIGN

A. Configuration of SOG

The effectiveness of the CMC structure has been verified by fabricating a SOG chip. Fig. 10 shows a configuration of the SOG employing the CMC. The p- and n-channel transistor pairs are arranged in 152 rows by 1324 columns. Macrocell columns, first-level wiring channels, and first-level power lines run vertically, while second-level power lines run horizontally. One BC is magnified in the center of Fig. 10.

TABLE II
FEATURES OF SOG CHIP

Technology	0.8μm CMOS Twin well structure
Gate length	0.8μm (LDD PMOS and NMOS)
Wiring pitch	2.4μm for Al1, Al2
Basic cell size	(38.4 x 3.6 μm²) x 8
2NAND gate delay	160 ps
Loaded gate delay	405 ps (2NAND, FO=3, Al=3mm)
Number of transistors	402,496
Number of raw gates	67 KG
Chip size	6 x 7 mm²



(a) (b)

Fig. 11. Delay characteristics of two-input NAND: (a) delay versus wiring length and (b) delay versus fan-out.

B. Features (Technology and Delay Characteristics)

Table II shows the features of the SOG master chip. A 0.8-μm CMOS technology is employed using LDD transistors in a twin-well structure combined with two layers of metallization. The physical gate length of both PMOS and NMOS transistors is 0.8 μm. The metallization pitch of both first- and second-level wiring is 2.4 μm. The size of one p- and n-channel transistor pair is 38.4×3.6 μm^2. The BC size is 38.4×28.8 μm^2.

Delay characteristics of internal gates are measured from ring oscillators implemented on the SOG chip. Fig. 11(a) and (b) shows the delay of two-input NAND as a function of wiring length and fan-out, respectively. A double-drive type gate is used to drive heavy loads. Two-input NAND unloaded delay is 160 ps. The loaded gate delay of the double-drive gate is 405 ps for two-input NAND with a fan-out of 3 and 3 mm of wiring.

There are 402 496 transistors, which is equivalent to 67 000 raw two-input NAND gates. The chip size is 6×7 mm^2.

VI. APPLICATION

A. 64-bit Multiplier

As an application, a 64-bit$\times$64-bit parallel multiplier employing the carry-save method has been implemented. Fig. 12 shows the block diagram of the multiplier which consists of two sets of 64-bit input registers, 4096 carry-save adders, 64 full adders, and 128-bit output registers. The full adder with two-input AND input, which is one of our macrocell libraries, is used for the carry-save adder. The complexity of the multiplier is 40 000 gates.

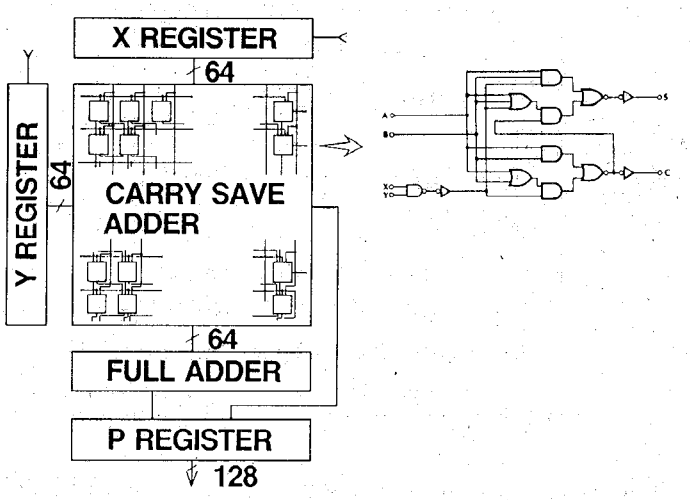


Fig. 12. Block diagram of 64×64-bit multiplier.

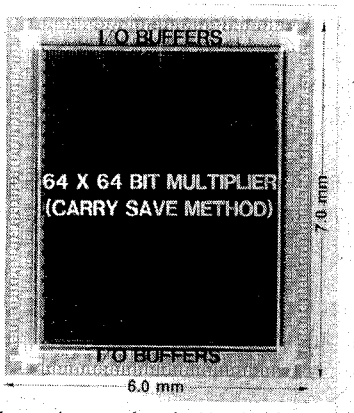


Fig. 13. Chip photomicrograph of 64×64-bit multiplier employing CMC structure. Chip size is 6×7 mm^2.

B. Chip Photomicrograph

Fig. 13 shows a photomicrograph of the multiplier laid out on the SOG master chip. The macrocell columns run vertically. There is no wide power bus. The chip size is 6×7 mm^2.

Fig. 14 is a photomicrograph showing a part of the multiplier using the CMC structure. Macrocell columns and first-level wiring run vertically. The width of the first-level wiring channels is adjusted so finely that unused wiring areas are minimized. Sufficient feedthrough wiring prevents local wiring congestion.

C. Layout Characteristics of Multiplier

Table III summarizes the layout characteristics of the multiplier by comparing them with the RMC case. CMC and RMC are defined as equal in both the p- and n-channel transistor-pair size of 38.4×3.6 μm^2 and the wiring pitch of 2.4 μm. The size of the core area is 5.88×4.82 mm^2 using the CMC. On the other hand, it is 9.19×4.82

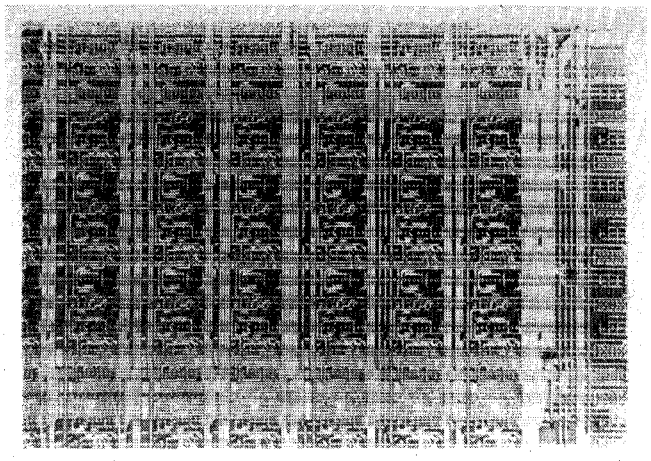


Fig. 14. Part of multiplier.

TABLE III
CHARACTERISTICS OF 64×64-BIT MULTIPLIER

	Column Macrocell	Row Macrocell
Core area	5.88 x 4.82 mm²	9.19 x 4.82 mm²
Gate utilization	60 %	38 %
Gate density	1,410 G/mm²	902 G/mm²
Ratio of wiring length	1	1.44
Multiplication time	100 ns	121 ns

mm^2 using the RMC. High gate utilization of 60 percent and gate density of 1410 G/mm^2 have been achieved. These values are 1.5 times greater than those of the RMC. Moreover, the improved CMC layout density reduces the net wiring length down to 70 percent of that in the conventional SOG. The total wiring length in the critical path is 127 and 229 mm in the CMC and RMC, respectively. As a result, fast multiplication time of 100 ns has been achieved, which is 83 percent compared with that of the RMC.

VII. SUMMARY

The CMC architecture has been proposed from our examination about the waste of silicon in the conventional SOG. The CMC provides three advantages in layout: continuous track allocation, sufficient feedthrough wiring, and fine mesh power distribution. The effectiveness of CMC has been verified by fabricating a 0.8-μm CMOS SOG chip. The 64-bit multiplier utilizing 40 000 gates has been full-automatically laid out using the CMC architecture on the 6×7-mm^2 SOG. High gate utilization of 60 percent and high gate density of 1410 G/mm^2 are obtained for the multiplier. Our layout results prove that the CMC architecture is effective in achieving higher gate density in CMOS SOG.

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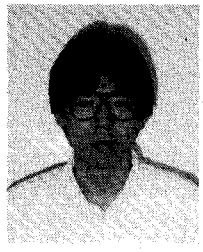
REFERENCES

[1] M. Takechi *et al.*, "A 630K transistor CMOS gate array," in *ISSCC Dig. Tech. Papers*, Feb. 1988, pp. 70–71.
[2] R. Blumberg *et al.*, "A 640K transistor sea-of-gates 1.2 micron HCMOS technology," in *ISSCC Dig. Tech. Papers*, Feb. 1988, pp. 74–75.
[3] M. Okabe *et al.*, "A CMOS sea-of-gates array with continuous track allocation," in *ISSCC Dig. Tech. Papers*, Feb. 1989, pp. 180–181.
[4] I. Ohkura *et al.*, "Gate isolation—A novel basic cell configuration for CMOS gate arrays," in *Proc. CICC*, May 1982, pp. 307–310.
[5] Y. Kuramitsu *et al.*, "A 540K-transistor CMOS variable-track masterslice," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 198–201, Apr. 1987.
[6] T. Wong *et al.*, "A high performance 129K gate CMOS gate array," in *Proc. CICC*, May 1986, pp. 568–571.
[7] T. Saigo *et al.*, "A triple-level wired 24K gate CMOS gate array," in *ISSCC Dig. Tech. Papers*, Feb. 1985, pp. 122–123.
[8] T. Kobayashi *et al.*, "DLM/TLM compatible 1.0 um gate array with over 100K usable gate," in *Proc. CICC*, May 1988, pp. 20.9.1–20.9.4.



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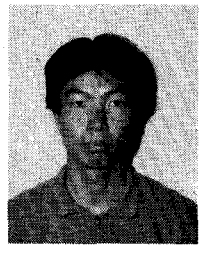

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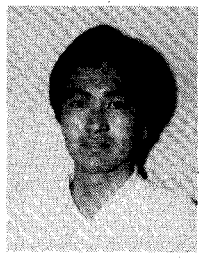

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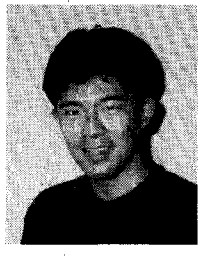

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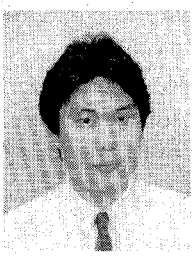

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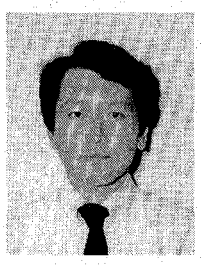
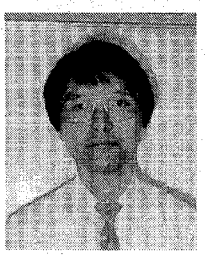


Tomoyoshi Noda was born in Tokyo, Japan, in 1957. He received the B.S. degree from the Faculty of Engineering, Waseda University, Tokyo, Japan, in 1980.

From 1980 to 1987 he was with the LSI Research and Development Laboratory, Mitsubishi Electric Corporation, Hyogo, Japan. Since 1986 he has been engaged in the research and development of computer-aided design associated with LSI at the ASIC Design Engineering Center, Mitsubishi Electric Corporation, Hyogo, Japan.

Mr. Noda is a member of the Institute of Electronics and Communication Engineers of Japan.



Masahiro Hatanaka was born in Hyogo, Japan, in 1952. He received the B.S. degree in physics from Kyoto University, Kyoto, Japan, in 1975.

He joined Kita-Itami Works, Mitsubishi Electronic Corporation, Hyogo, Japan, in 1975. From 1975 to 1982 he was engaged in the wafer process engineering of MOS VLSI. Since 1982 he has been working on the development of process technologies at the Mitsubishi LSI Research and Development Laboratory, Hyogo, Japan.

Yoichi Kuramitsu (M'84), for photograph and biography please see this issue, p. 1279.