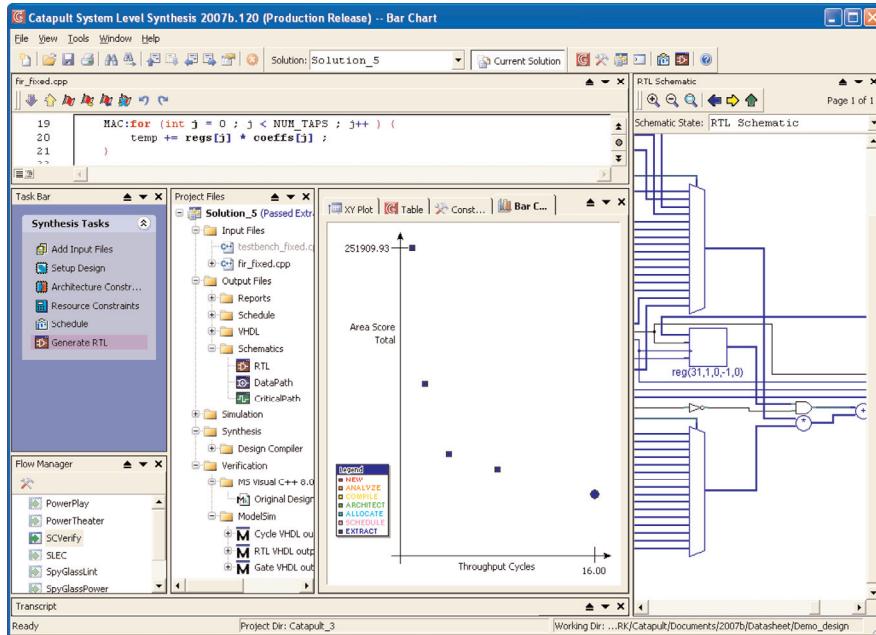


Catapult C Synthesis

D A T A S H E E T



Catapult C Synthesis offers a quick and easy path from abstract C specifications to high-quality hardware implementations.

The Fastest Path to Verified RTL

Traditional hardware design methods require hand written RTL development and debugging and are too time consuming for today's complex digital applications. The Catapult® Synthesis tool suite is the only product to synthesize full hierarchical systems comprised of both control blocks and algorithmic units from pure C++. Its unique decoupling control channel (DCC) technology combined with a patent-pending verification flow form the key technological components of a unified flow for modelling, synthesizing and verifying the complex mix of blocks commonly found in sophisticated applications. Further more, advanced power optimizations such as multi-clock gating provide significant reductions in dynamic power consumption. This enables rapid design and verification of complex, high-performance ASIC and FPGA hardware needed in wireless, satellite, video, and image processing applications. At the end of 2008, over 100 million ASICs had shipped with hardware designed using Catapult.

Catapult C Synthesis Product Family

The Catapult product family was the first to synthesize industry-standard ANSI C++, safely generating verified RTL 10-20x faster than other methods. Unlike RTL methodologies or other high-level synthesis (HLS) tools, which require extensive hardware detail to be hard-coded into the source, Catapult uses automation to avoid hand-coded design errors and rapidly find the best implementation for performance, area or power.

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Major product features

- Synthesizes pure ANSI C++ with no proprietary extensions
- Optimizes for performance, area and power
- Design and verify mixed datapath and control
- ASIC and FPGA technology aware scheduling for high performance hardware
- Incremental design methodology allows maximum visibility, maximum user control and fastest path to hardware
- Interface optimization through patent-pending interface synthesis
- ANSI C++ testbench reuse for automatic RTL verification with SystemC transactor generation
- SystemC TLM generation for faster system verification and connection to SystemC design flows
- Automatically generates RTL meaning no bugs typically found with manual methods
- Supports bit-accurate data types for bit-true simulation up to 10,000x faster than RTL
- Hierarchical design support for synthesizing pipelined, multi-block subsystems from ANSI C++
- Precise library modeling accurately predicts area and delay up front, without costly RTL synthesis runtimes
- Tight integration with RTL synthesis yields rapid timing closure
- Graphic display of design bottlenecks and inefficiencies in the hierarchical Gantt chart
- Multi-view cross-probing between Gantt chart, source code and schematic

Micro-Architecture Analysis and Optimization

Traditional methods require such labor intensive design and verification flows that they leave minimal, if any, time for evaluating alternate micro-architectures. As a result, hardware designers are forced to limit their selection, which often results in non-optimal hardware. Automating RTL creation with Catapult enables the designer to easily explore a wide range of alternative micro-architectures for a given design. Catapult gives designers superior control, generating solutions based on user constraints and graphically displaying the results in a choice of X-Y plots, bar charts, tabular and schematic views. Users quickly make informed decisions in terms of power, area and performance to deliver optimal hardware results.

The hierarchical Gantt chart in Catapult provides information on critical paths, data flow and component utilization. It gives designers immediate insight into hard-coded performance bottlenecks and inefficiencies such as memory bandwidth limitations, loop dependencies that prevent parallelism and data dependencies that limit optimal scheduling. The designer can quickly identify problem areas and cross probe back to the C++ code to understand and optimize both the source and hardware implementation, quickly converging on an optimal hardware implementation.

Interface Synthesis

Compared to other high-level synthesis tools, Catapult does not require interface protocols to be embedded in the source description. Rather, it accepts a pure ANSI C++ description as its input, and uses patent-pending interface synthesis technology to control the timing and communications protocol on the design interface. This enables interface analysis so designers can explore a full range of hardware interface options such as streaming, single- or dual-port RAM, hand-shaking, FIFO, AMBA and many other built-in I/O components. Users can also target custom or proprietary I/O components using the Catapult Library Builder tool.

Hierarchical Design Synthesis

Catapult C Synthesis is the first high-level synthesis tool to synthesize multi-block pipelined and concurrent hierarchical designs from pure sequential ANSI C++. Adding hierarchy can not only improve the performance of the design, but also can significantly reduce the time required for synthesis, which greatly increases the efficiency of creating and veri-

fying these complex designs. At the start of the design, Catapult C Synthesis assists the designer in identifying and analyzing possible hierarchy, allowing the user to interactively select the optimal hierarchy structure. Once the designer determines the appropriate level of hierarchy, Catapult uses its hierarchical engine to synthesize each functions to concurrent hierarchical blocks with autonomous FSM, control logic and datapaths. In tandem, the tool's robust channel synthesis allows the user to optimize inter-block communication supporting streamed channels with FIFOs, ping-pong memories, shared memories, channel depth and channel width. Catapult can also perform top-level pipelining automatically building concurrent and pipelined sub-blocks to satisfy the top level throughput constraint.

SystemC Verification Environment

Catapult provides integrated block-level verification environment by generating SystemC transactors that synchronize timed RTL with a transaction or sequential test environment. This connection allows designers to reuse the original C test-bench to functionally verify the RTL design against the C description. This flow is also able to re-play the cycle-accurate behavior of the RTL back into the original C design letting designers analyze timing related aspects directly in the untimed C++ source.

Low-Power Exploration and Optimization

Catapult C Synthesis fully automates highly efficient low-power design techniques such as multi-level clock gating. The tool will thoroughly analyze and optimize RTL netlists to reduce power consumption, working on a per-register basis to maximize power savings. These powerful optimizations can be used in combination with Catapult C's power exploration flow, letting designers instantly generate dozens of implementation candidates, sweeping design parameters such as clock frequency, performance and micro-architecture. With those design options at hand, engineers can easily pick the solution best fitting their best power/performance/area requirements. This unique combination of power exploration and optimization delivers unrivalled results, dramatically cooling down the powermeter.

Comprehensive Design Constraints

Synthesis provides complete control over how a design is synthesized to hardware. From the same source, hardware designers use high-level constraints to create compact to highly parallel implementations. The architectural constraints

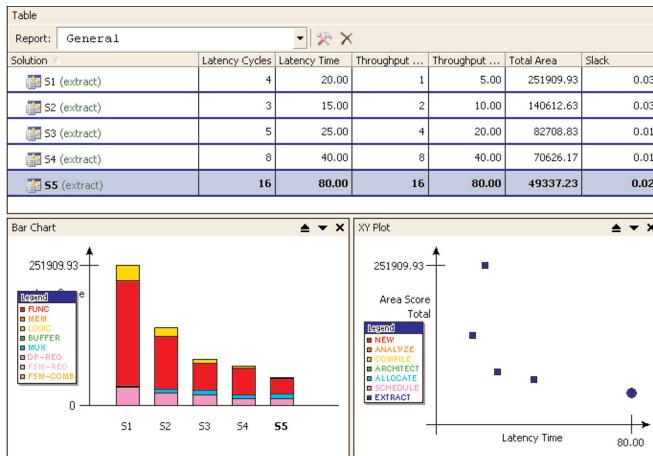


Figure 2: X-Y plot, Bar Chart, and Table views provide feedback to help compare and contrast metrics of all solutions.

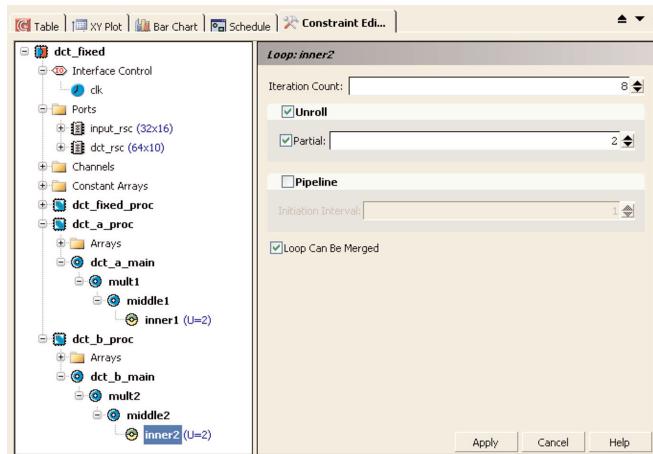


Figure 3: You can optimize hardware by applying architectural constraints to unroll, merge and pipeline loops, map arrays to RAMs, and control resource allocation.

window presents a graphical view of all ports, arrays, and loops in the design, and allows any or all of the following high-level constraints to be applied:

- Loop merging, unrolling and pipelining
- Relative cycle-by-cycle timing
- RAM, ROM, or FIFO array mapping
- Memory resources merging
- Memory width re-sizing

Catapult combines automation with specific high-level constraints so the user can precisely control the hardware implementation to interactively converge on significantly better quality designs in far less time.

Predictable Timing Closure

Catapult maximizes design performance by structuring essential FSM control logic off the timing-critical data path. Catapult constructs highly optimized data paths by leveraging the native technology-specific operators used by the downstream RTL synthesis tools such as DesignWare for Design Compiler. This methodology ensures precise knowledge of data path delays leading to correct-by-construction timing through RTL and physical synthesis.

Integrated Flows

Catapult produces RTL netlists in VHDL and Verilog along with simulation and synthesis scripts for leading tools such as Design Compiler®, Precision® Synthesis, Questa™, and more. The tool also takes advantage of RTL synthesis features like automatic RAM or DSP macro inferencing. To ensure users can create the best design possible, Catapult offers established flows for sequential verification and power estimation through close partnership with leading 3rd party providers. The sequential equivalence checking flow proves functional equivalence between system-level input models and the output RTL designs, providing formal proof between pure ANSI C++ source and RTL output. The power optimization and estimation flows can be leveraged by designers to target power-aware applications such as consumer products and mobile communications.

Carry-save Adder Optimization

Catapult also implements carry-save adder, an optimization for streamlining computations and throughput across large adder trees. Carry-save adder optimization enables Catapult to create higher-performance hardware blocks while decreasing hardware size.

Advanced Resource Management

Catapult C Synthesis offers additional user control and optimization capabilities with fine-grain resource management. Users can control the specific architectures and quantities of components helping to improve design area by up to 15 percent and design speed by up to five percent.

SystemC Transaction Level Model (TLM) Generation

Catapult provides integrated verification for system designers working in a SystemC environment by generating a SystemC transaction level model (TLM) for both

transaction and pin-accurate simulation. These higher abstraction models allow a single SystemC-based testing environment for the entire system that is optimized to simulate 20 to 100 times faster than RTL.

Catapult C Library Builder

Catapult C Library Builder collects detailed characterization data from the downstream RTL synthesis tools with specific target technology libraries. This allows Catapult to precisely schedule hardware resources, chain operators, infer multi-cycle components, and quickly provide accurate area, latency, and throughput estimates without spending costly time and effort going through RTL synthesis. Catapult Library Builder also allows designers to leverage custom components including memories, IP, DesignWare, and existing RTL.

Customer-Proven C Synthesis

Catapult has already been instrumental in many successful ASIC tapeouts and FPGA designs from major hardware design companies worldwide. The mature, third generation C synthesis environment automatically generates error-free RTL from pure ANSI C++ up to 20x faster than traditional

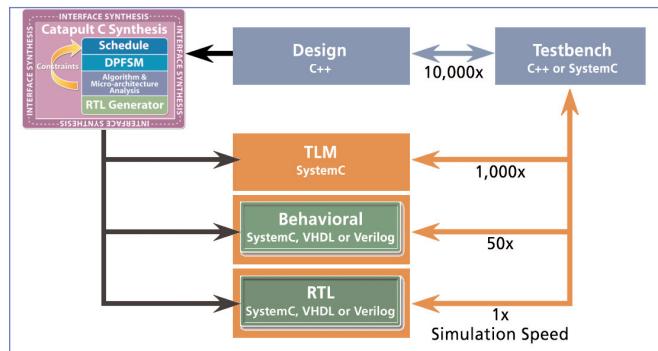


Figure 4: Catapult C supports SystemC transaction level systems by generating transactors that synchronize timed RTL with a transaction or sequential test environment. This connection allows a single SystemC-based testing environment for the entire design flow.

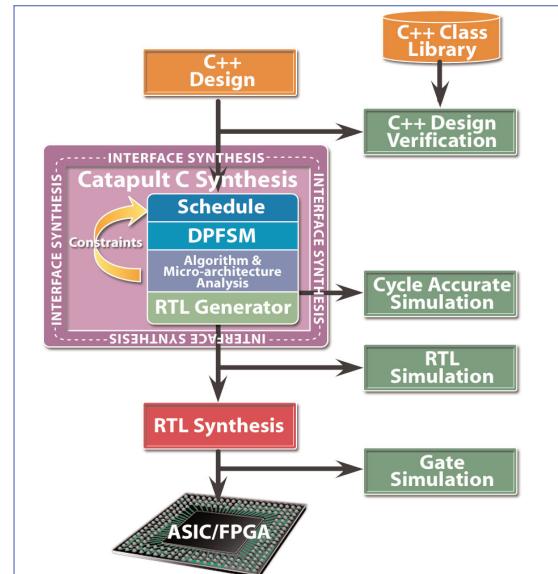


Figure 5: The Catapult design flow gives you the opportunity to evaluate a wider range of micro-architecture than previously possible using hand-coded methods.

manual methods. Using industry standard pure ANSI C++ to describe functional intent, designers move up to a more productive abstraction level for designing complex hardware typically found in modern applications. The tool's advanced analysis allows hardware designers to fully and interactively explore the micro-architecture and interface design space, yielding high-performance hardware that rivals hand-coded design quality. Catapult unites two distinct domains - system-level design and hardware design - and when combined with Mentor Graphics Questa simulation tools, lays the foundation for next-generation electronic system level (ESL) design.

Platforms Supported

Windows NT/2000/XP, Linux RedHat Enterprise and SUN Solaris 8.

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