

# Chapter 31 Multilevel Power Converters

*Surin Khomfoi and Leon M. Tolbert*

*The University of Tennessee*

## 31.1 Introduction

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application [1-3].

The concept of multilevel converters has been introduced since 1975 [4]. The term multilevel began with the three-level converter [5]. Subsequently, several multilevel converter topologies have been developed [6-13]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

- *Staircase waveform quality*: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the  $dv/dt$  stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.
- *Common-mode (CM) voltage*: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [14].
- *Input current*: Multilevel converters can draw input current with low distortion.
- *Switching frequency*: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Unfortunately, multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex.

Plentiful multilevel converter topologies have been proposed during the last two decades. Contemporary research has engaged novel converter topologies and unique modulation schemes. Moreover, three different major multilevel converter structures have been reported in the literature: cascaded H-bridges converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped). Moreover, abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In addition, many multilevel converter applications focus on industrial medium-voltage motor drives [11, 15, 16], utility interface for renewable energy systems [17], flexible AC transmission system (FACTS) [18], and traction drive systems [19].

This chapter reviews state of the art of multilevel power converter technology. Fundamental multilevel converter structures and modulation paradigms are discussed including the pros and cons of each technique. Particular concentration is addressed in modern and more practical industrial applications of multilevel converters. A procedure for calculating the required ratings for the active switches, clamping diodes, and dc link capacitors including a design example are described. Finally, the possible future developments of multilevel converter technology are noted.

## 31.2 Multilevel power converter structures

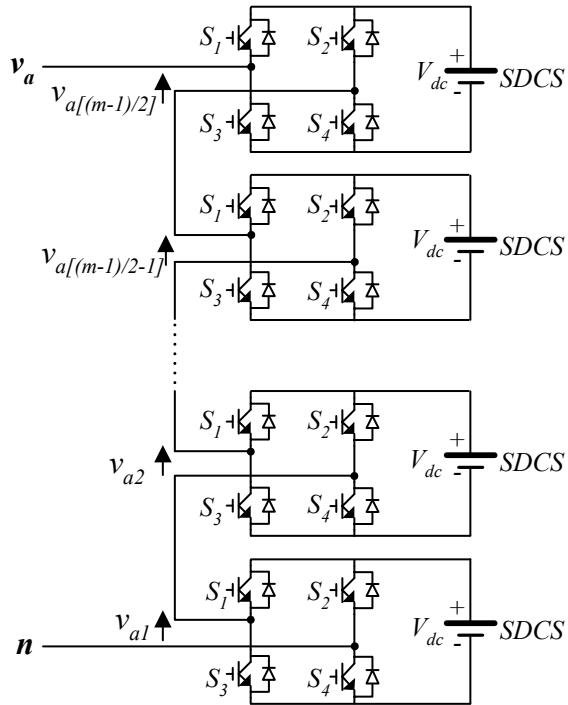
As previously mentioned, three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. Before continuing discussion in this topic, it should be noted that the term *multilevel converter* is utilized to refer to a power electronic circuit that could operate in an inverter or rectifier mode. The multilevel inverter structures are the focus of in this chapter; however, the illustrated structures can be implemented for rectifying operation as well.

### 31.2.1 Cascaded H-Bridges

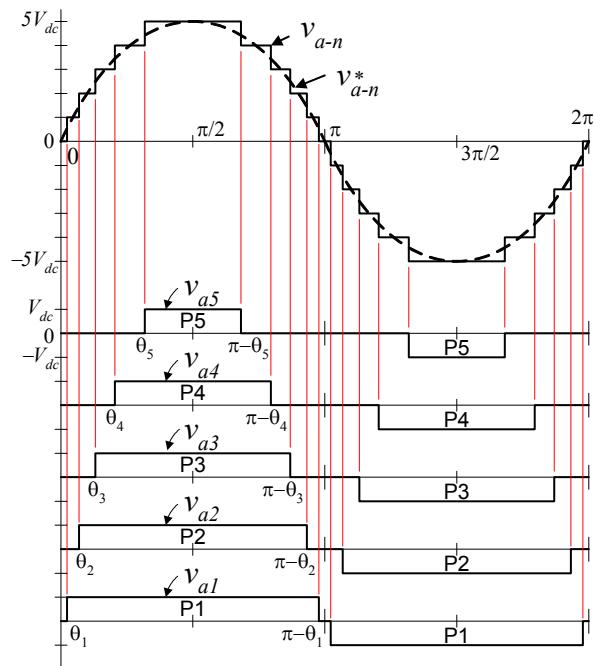
A single-phase structure of an  $m$ -level cascaded inverter is illustrated in Figure 31.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs,  $+V_{dc}$ ,  $0$ , and  $-V_{dc}$  by connecting the dc source to the ac output by different combinations of the four switches,  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ . To obtain  $+V_{dc}$ , switches  $S_1$  and  $S_4$  are turned on, whereas  $-V_{dc}$  can be obtained by turning on switches  $S_2$  and  $S_3$ . By turning on  $S_1$  and  $S_2$  or  $S_3$  and  $S_4$ , the output voltage is  $0$ . The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels  $m$  in a cascade inverter is defined by  $m = 2s+1$ , where  $s$  is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 31.2. The phase voltage  $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$ .

For a stepped waveform such as the one depicted in Figure 31.2 with  $s$  steps, the Fourier Transform for this waveform follows [15,19]:

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n \left[ \cos(n\theta_1) + \cos(n\theta_2) + \dots + \cos(n\theta_s) \right] \frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1, 3, 5, 7, \dots \quad (31.1)$$



**Figure 31.1.** Single-phase structure of a multilevel cascaded H-bridges inverter.



**Figure 31.2.** Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

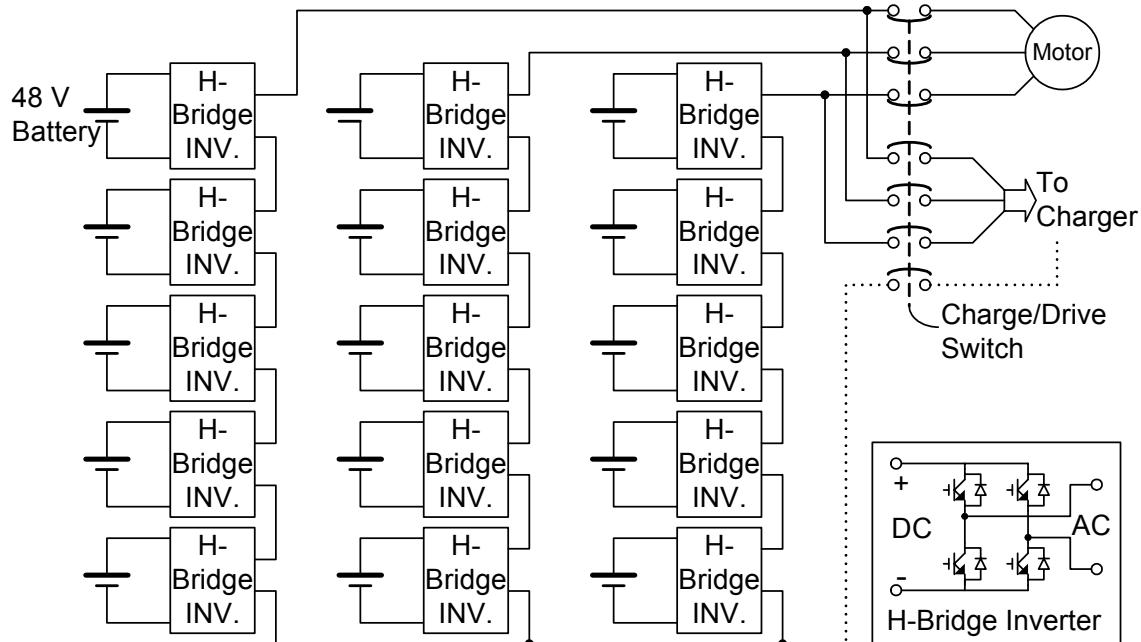
From (31.1), the magnitudes of the Fourier coefficients when normalized with respect to  $V_{dc}$  are as follows:

$$H(n) = \frac{4}{\pi n} [\cos(n\theta_1) + \cos(n\theta_2) + \dots + \cos(n\theta_s)], \quad \text{where } n = 1, 3, 5, 7, \dots \quad (31.2)$$

The conducting angles,  $\theta_1, \theta_2, \dots, \theta_s$ , can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13<sup>th</sup>, harmonics are eliminated [25]. More detail on harmonic elimination techniques will be presented in the next section.

Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure 31.3, or in delta. Peng has demonstrated a prototype multilevel cascaded static var generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system [20-23]. The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected. Peng [20] and Joos [24] have also shown that a cascade inverter can be directly connected in series with the electrical system for static var compensation. Cascaded inverters are ideal for connecting renewable energy sources with an ac grid, because of the need for separate dc sources, which is the case in applications such as photovoltaics or fuel cells.

Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultracapacitors are well suited to serve as SDCSs [19, 26]. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Figure 31.3. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.



**Figure 31.3.** Three-phase wye-connection structure for electric vehicle motor drive and battery charging.

Manjrekar has proposed a cascade topology that uses multiple dc levels, which instead of being identical in value are multiples of each other [27-28]. He also uses a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical, modular units for each level.

The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows [29, 30].

*Advantages:*

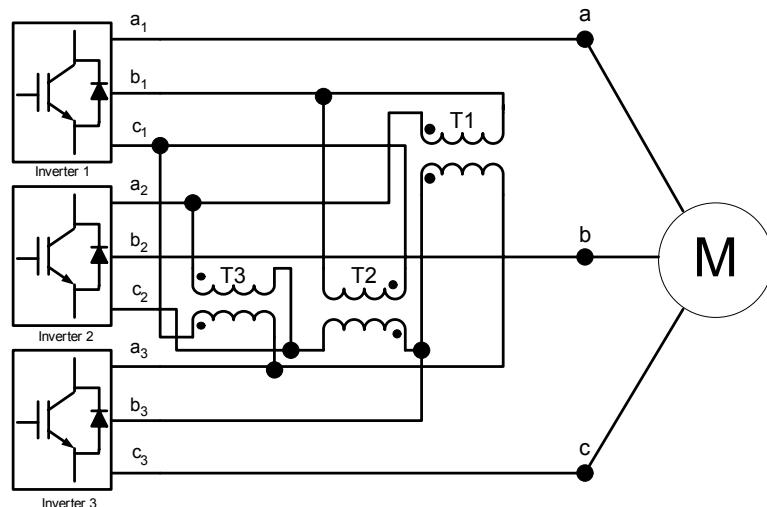
- The number of possible output voltage levels is more than twice the number of dc sources ( $m = 2s + 1$ ).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

*Disadvantages:*

- Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

Another kind of cascaded multilevel converter with transformers using standard three-phase bi-level converters has been proposed [14]. The circuit is shown in Figure 31.4. The converter uses output transformers to add different voltages. In order for the converter output voltages to be added up, the outputs of the three converters need to be synchronized with a separation of  $120^\circ$  between each phase. For example, obtaining a three-level voltage between outputs  $a$  and  $b$ , the output voltage can be synthesized by  $V_{ab} = V_{a1-b1} + V_{b1-a2} + V_{a2-b2}$ . An isolated transformer is used to provide voltage boost. With three converters synchronized, the voltages  $V_{a1-b1}$ ,  $V_{b1-a2}$ ,  $V_{a2-b2}$ , are all in phase; thus, the output level can be tripled [1].

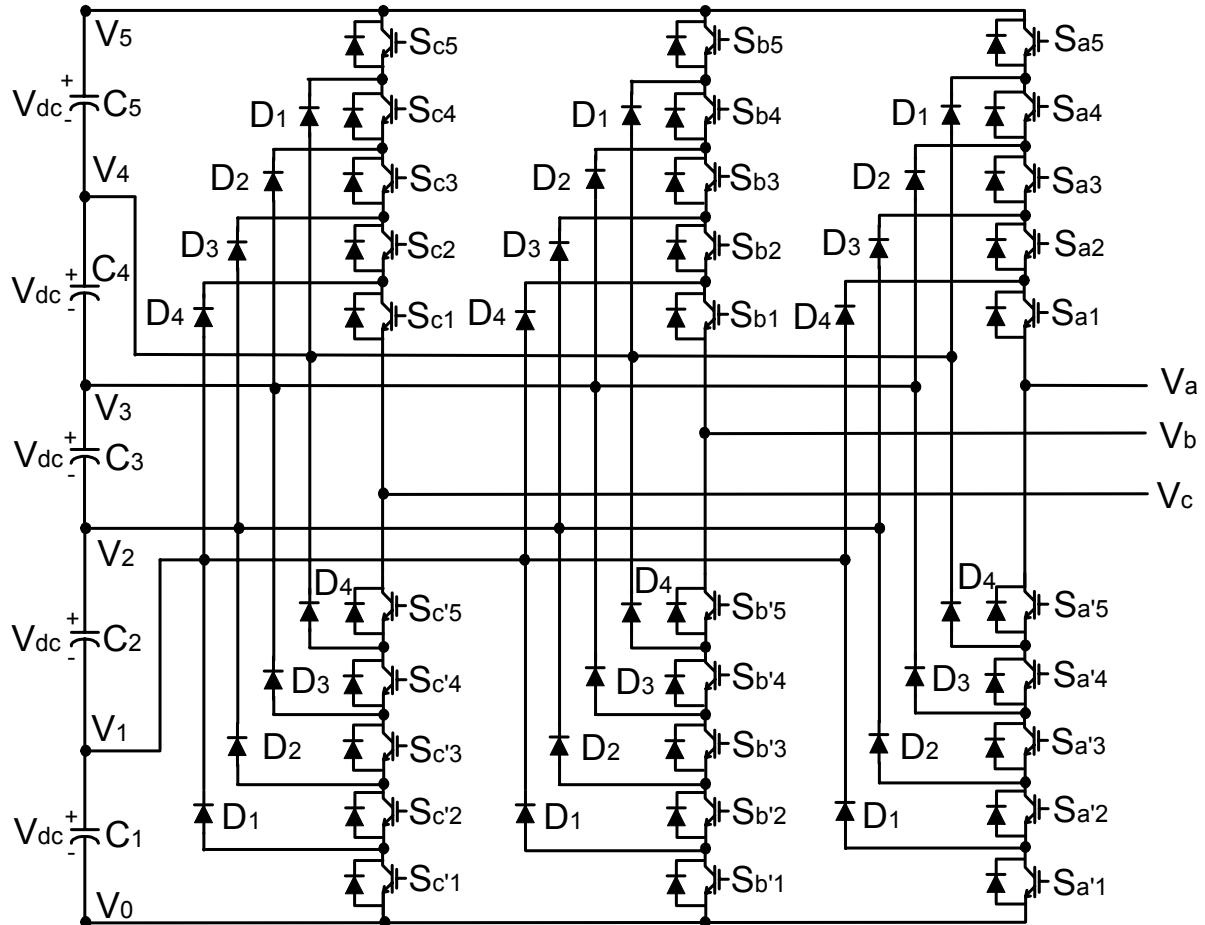
The advantage of the cascaded multilevel converters with transformers using standard three-phase bi-level converters is the three converters are identical and thus control is more simple. However, the three converters need separate DC sources, and a transformer is needed to add up the output voltages.



**Figure 31.4.** Cascaded multilevel converter with transformers using standard three-phase bi-level converters.

### 31.2.2 Diode-Clamped Multilevel Inverter

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [5]. In the 1990s several researchers published articles that have reported experimental results for four-, five-, and six-level diode-clamped converters for such uses as static var compensation, variable speed motor drives, and high-voltage system interconnections [18-31]. A three-phase six-level diode-clamped inverter is shown in Figure 31.5. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is  $V_{dc}$ , and the voltage stress across each switching device is limited to  $V_{dc}$  through the clamping diodes. Table 31.1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage  $V_0$  as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg  $a$  are  $(S_{a1}, S_{a'1})$ ,  $(S_{a2}, S_{a'2})$ ,  $(S_{a3}, S_{a'3})$ ,  $(S_{a4}, S_{a'4})$ , and  $(S_{a5}, S_{a'5})$ . Table 31.1 also shows that in a diode-clamped inverter, the switches that are on for a particular phase leg are always adjacent and in series. For a six-level inverter, a set of five switches is on at any given time.



**Figure 31.5.** Three-phase six-level structure of a diode-clamped inverter.

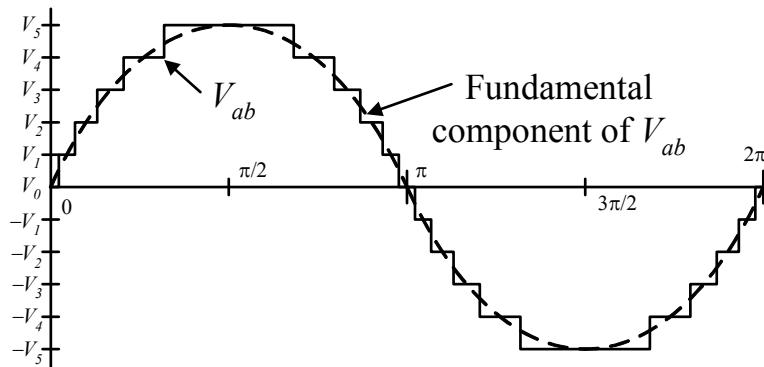
Table 31.1. Diode-clamped six-level inverter voltage levels and corresponding switch states.

Voltage $V_{a0}$	Switch State									
	$S_{a5}$	$S_{a4}$	$S_{a3}$	$S_{a2}$	$S_{a1}$	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5Vdc$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4Vdc$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3Vdc$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2Vdc$	0	0	0	1	1	1	1	1	0	0
$V_1 = Vdc$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

Figure 31.6 shows one of the three line-line voltage waveforms for a six-level inverter. The line voltage  $V_{ab}$  consists of a phase-leg  $a$  voltage and a phase-leg  $b$  voltage. The resulting line voltage is an 11-level staircase waveform. This means that an  $m$ -level diode-clamped inverter has an  $m$ -level output phase voltage and a  $(2m-1)$ -level output line voltage.

Although each active switching device is required to block only a voltage level of  $V_{dc}$ , the clamping diodes require different ratings for reverse voltage blocking. Using phase  $a$  of Figure 31.5 as an example, when all the lower switches  $S_{a'1}$  through  $S_{a'5}$  are turned on,  $D_4$  must block four voltage levels, or  $4V_{dc}$ . Similarly,  $D_3$  must block  $3V_{dc}$ ,  $D_2$  must block  $2V_{dc}$ , and  $D_1$  must block  $V_{dc}$ . If the inverter is designed such that each blocking diode has the same voltage rating as the active switches,  $D_n$  will require  $n$  diodes in series; consequently, the number of diodes required for each phase would be  $(m-1) \times (m-2)$ . Thus, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter [30].

One application of the multilevel diode-clamped inverter is an interface between a high-voltage dc transmission line and an ac transmission line [30]. Another application would be as a variable speed drive for high-power medium-voltage (2.4 kV to 13.8 kV) motors as proposed in [3, 6, 25, 29-31]. Static var compensation is an additional function for which several authors have proposed for the diode-clamped converter. The main advantages and disadvantages of multilevel diode-clamped converters are as follows [1- 3]:



**Figure 31.6.** Line voltage waveform for a six-level diode-clamped inverter.

Advantages:

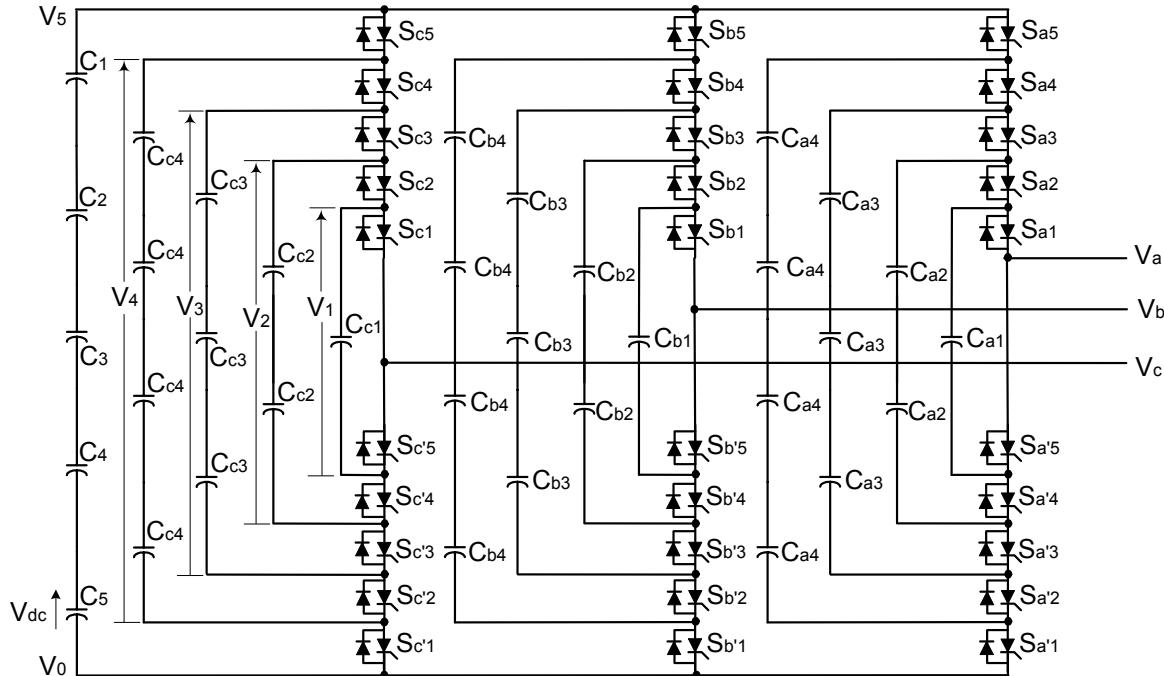
- All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.
- The capacitors can be pre-charged as a group.
- Efficiency is high for fundamental frequency switching.

Disadvantages:

- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

### 31.2.3 Flying Capacitor Multilevel Inverter

Meynard and Foch introduced a flying-capacitor-based inverter in 1992 [32]. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the flying capacitor multilevel inverter is shown in Figure 31.7. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.



**Figure 31.7.** Three-phase six-level structure of a flying capacitor inverter.

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Table 31.2 shows a list of all the combinations of phase voltage levels that are possible for the six-level circuit shown in Figure 31.7. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has *phase* redundancies, whereas the diode-clamped inverter has only *line-line* redundancies [2, 3, 33]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

In addition to the  $(m-1)$  dc link capacitors, the  $m$ -level flying-capacitor multilevel inverter will require  $(m-1) \times (m-2)/2$  auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. One application proposed in the literature for the multilevel flying capacitor is static var generation [2, 3]. The main advantages and disadvantages of multilevel flying capacitor converters are as follows [2, 3].

*Advantages:*

- Phase redundancies are available for balancing the voltage levels of the capacitors.
- Real and reactive power flow can be controlled.
- The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

*Disadvantages:*

- Control is complicated to track the voltage levels for all of the capacitors. Also, precharging all of the capacitors to the same voltage level and startup are complex.
- Switching utilization and efficiency are poor for real power transmission.
- The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

### 31.2.4 Other Multilevel Inverter Structures

Besides the three basic multilevel inverter topologies previously discussed, other multilevel converter topologies have been proposed; however, most of these are “hybrid” circuits that are combinations of two of the basic multilevel topologies or slight variations to them. Additionally, the combination of multilevel power converters can be designed to match with a specific application based on the basic topologies. In the interest of completeness, some of these will be identified and briefly described.

**Table 31.2.** Flying-capacitor six-level inverter redundant voltage levels and corresponding switch states.

Voltage $V_{a0}$	Switch State									
	$S_{a5}$	$S_{a4}$	$S_{a3}$	$S_{a2}$	$S_{a1}$	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_{a0} = 5V_{dc}$ (no redundancies)										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_{a0} = 4V_{dc}$ (4 redundancies)										
$5V_{dc} - V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc} - 3V_{dc} + 2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc} - 2V_{dc} + V_{dc}$	1	1	1	0	1	0	0	0	1	0
$V_{a0} = 3V_{dc}$ (5 redundancies)										
$5V_{dc} - 2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc} - V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc} - V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc} - 3V_{dc} + V_{dc}$	1	1	0	0	1	0	0	1	1	0
$4V_{dc} - 2V_{dc} + V_{dc}$	0	1	1	0	1	1	0	0	1	0
$V_{a0} = 2V_{dc}$ (6 redundancies)										
$5V_{dc} - 3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc} - 4V_{dc} + V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc} - 2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc} - 3V_{dc} + V_{dc}$	0	1	0	0	1	1	0	1	1	0
$3V_{dc} - V_{dc}$	0	0	1	1	0	1	1	0	0	1
$3V_{dc} - 2V_{dc} + V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_{a0} = V_{dc}$ (4 redundancies)										
$5V_{dc} - 4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc} - 3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc} - 2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc} - V_{dc}$	0	0	0	1	0	1	1	1	0	1
$V_{dc}$	0	0	0	0	1	1	1	1	1	0
$V_{a0} = 0$ (no redundancies)										
0	0	0	0	0	0	1	1	1	1	1

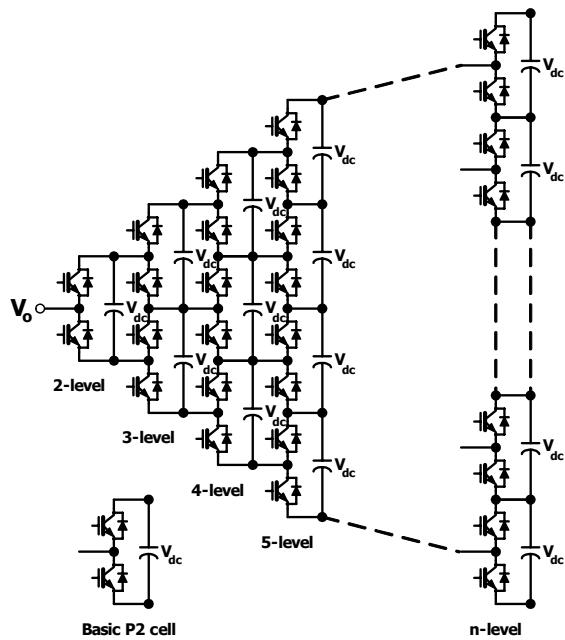
#### A. Generalized Multilevel Topology

Existing multilevel converters such as diode-clamped and capacitor-clamped multilevel converters can be derived from the generalized converter topology called *P2* topology proposed by Peng [34] as illustrated in Figure 31.8. The generalized multilevel converter topology can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion and without any assistance from other circuits at any number of levels automatically. Thus, the topology provides a complete multilevel topology that embraces the existing multilevel converters in principle.

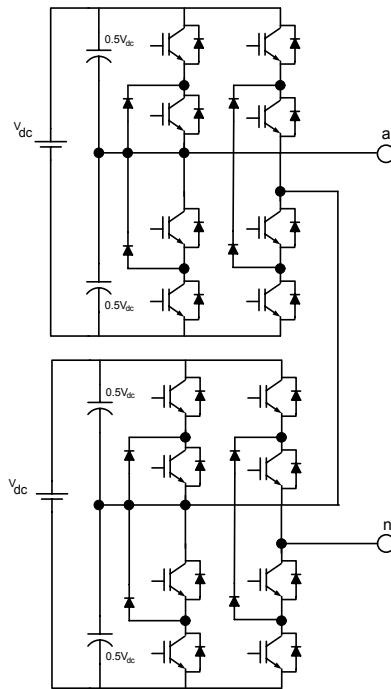
Figure 31.8 shows the *P2* multilevel converter structure per phase leg. Each switching device, diode, or capacitor's voltage is  $1V_{dc}$ , for instance,  $1/(m-1)$  of the DC-link voltage. Any converter with any number of levels, including the conventional bi-level converter can be obtained using this generalized topology [1, 34].

#### B. Mixed-Level Hybrid Multilevel Converter

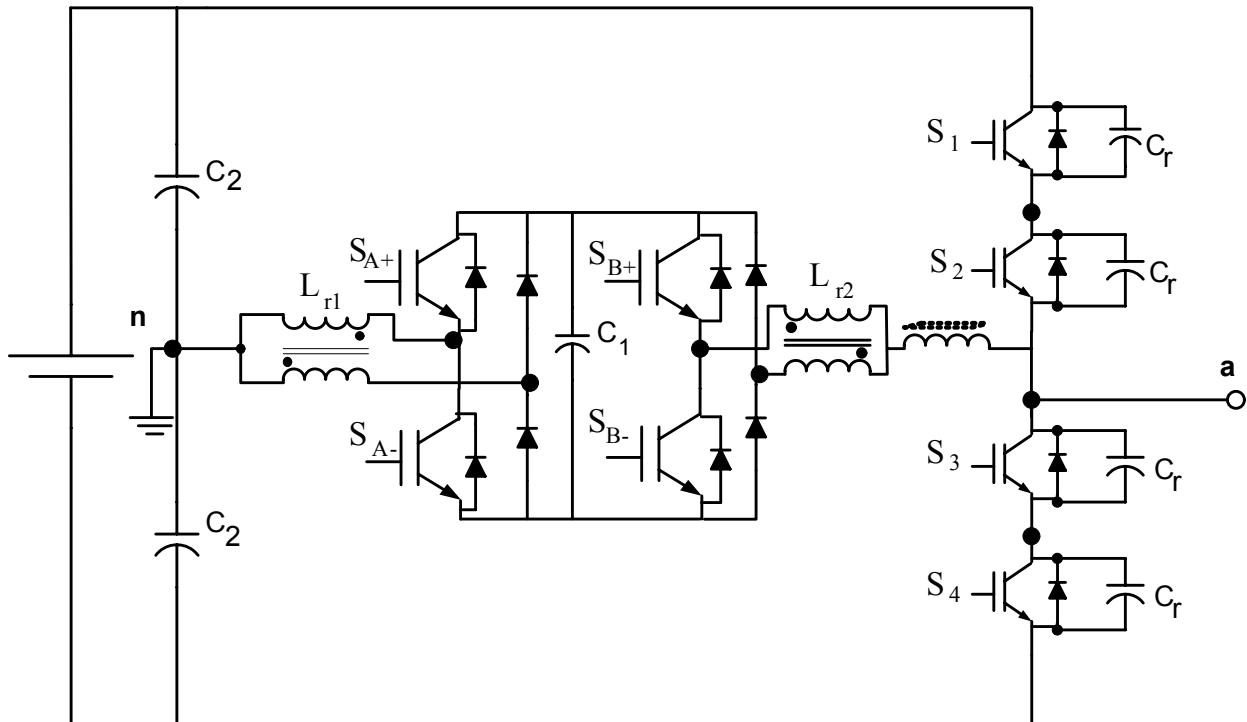
To reduce the number of separate DC sources for high-voltage, high-power applications with multilevel converters, diode-clamped or capacitor-clamped converters could be used to replace the full-bridge cell in a cascaded converter [35]. An example is shown in Figure 31.9. The nine-level cascade converter incorporates a three-level diode-clamped converter as the cell. The original cascaded H-bridge multilevel converter requires four separate DC sources for one phase leg and twelve for a three-phase converter. If a five-level converter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate DC sources are needed for one phase leg and six for a three-phase converter. The configuration has mixed-level hybrid multilevel units because it embeds multilevel cells as the building block of the cascade converter. The advantage of the topology is it needs less separate DC sources. The disadvantage for the topology is its control will be complicated due to its hybrid structure.



**Figure 31.8** Generalized *P2* multilevel converter topology for one phase leg.



**Figure 31.9** Mixed-level hybrid unit configuration using the three-level diode-clamped converter as the cascaded converter cell to increase the voltage levels.



**Figure 31.10** Zero-voltage switching capacitor-clamped inverter circuit.

### C. Soft-Switched Multilevel Converter

Some soft-switching methods can be implemented for different multilevel converters to reduce the switching loss and to increase efficiency. For the cascaded converter, because each converter cell is a bi-level circuit, the implementation of soft switching is not at all different from that of conventional bi-level converters. For capacitor-clamped or diode-clamped converters, soft-switching circuits have been proposed with different circuit combinations. One of soft-switching circuits is a zero-voltage-switching type which includes auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations [1, 36] as shown in Figure 31.10.

### D. Back-to-Back Diode-Clamped Converter

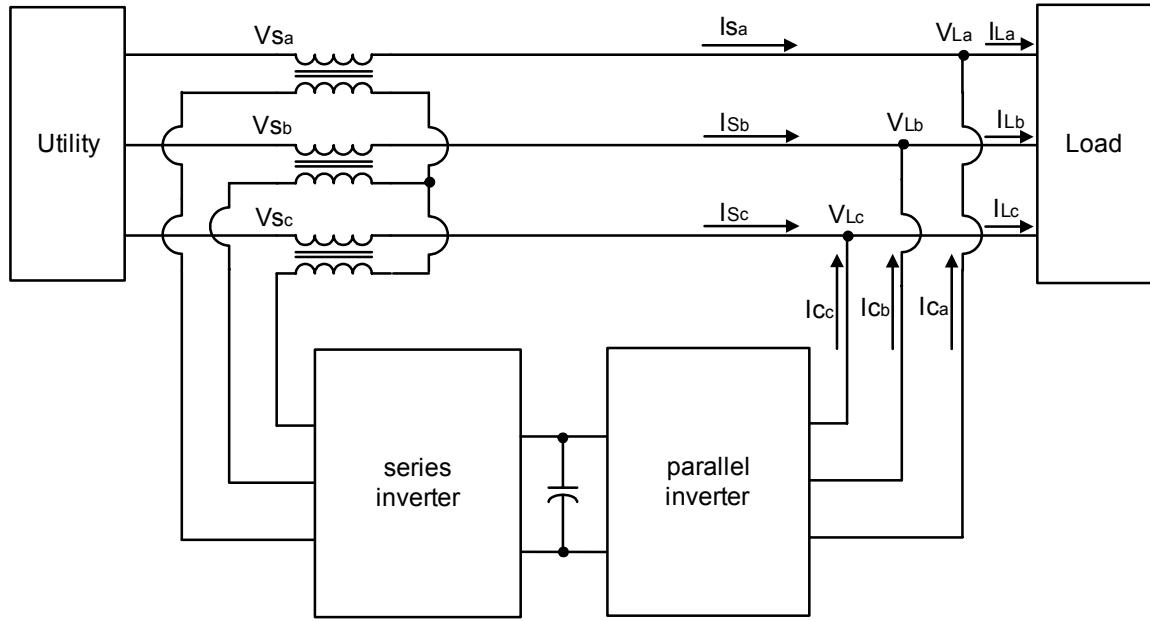
Two multilevel converters can be connected in a back-to-back arrangement and then the combination can be connected to the electrical system in a series-parallel arrangement as shown in Figure 31.11. Both the current demanded from the utility and the voltage delivered to the load can be controlled at the same time. This series-parallel active power filter has been referred to as a universal power conditioner [37-43] when used on electrical distribution systems and as a universal power flow controller [44-48] when applied at the transmission level. Previously, Lai and Peng [30] proposed the back-to-back diode-clamped topology shown in Figure 31.12 for use as a high-voltage dc inter connection between two asynchronous ac systems or as a rectifier/inverter for an adjustable speed drive for high-voltage motors. The diode-clamped inverter has been chosen over the other two basic multilevel circuit topologies for use in a universal power conditioner for the following reasons:

- All six phases (three on each inverter) can share a common dc link. Conversely, the cascade inverter requires that each dc level be separate, and this is not conducive to a back-to-back arrangement.
- The multilevel flying-capacitor converter also shares a common dc link; however, each phase leg requires several additional auxiliary capacitors. These extra capacitors would add substantially to the cost and the size of the conditioner.

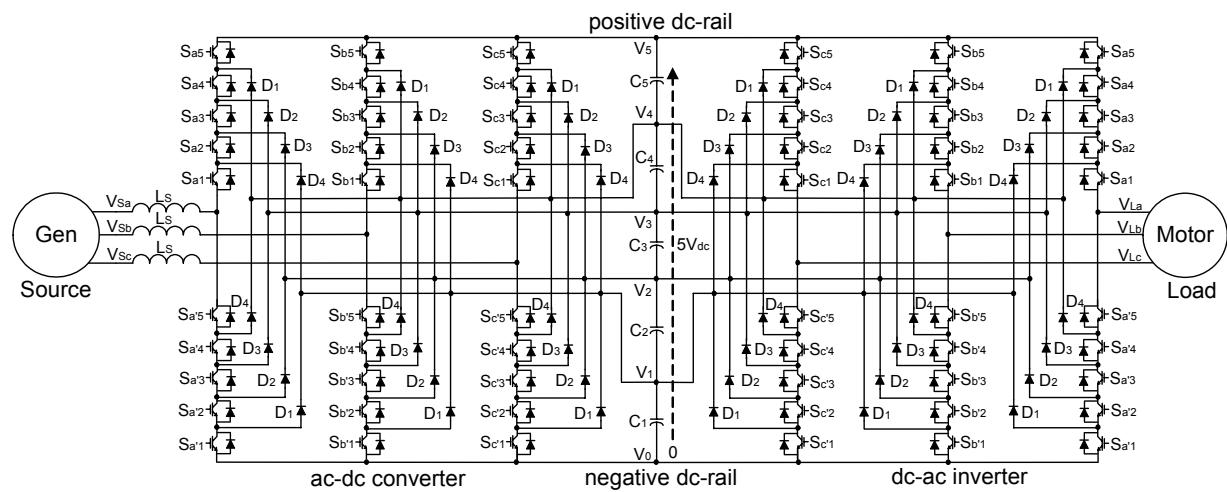
Because a diode-clamped converter acting as a universal power conditioner will be expected to compensate for harmonics and/or operate in low amplitude modulation index regions, a more sophisticated, higher-frequency switch control than the fundamental frequency switching method will be needed. For this reason, multilevel space vector and carrier-based PWM approaches are compared in the next section, as well as novel carrier-based PWM methodologies.

## 31.3 Multilevel Converter PWM Modulation Strategies

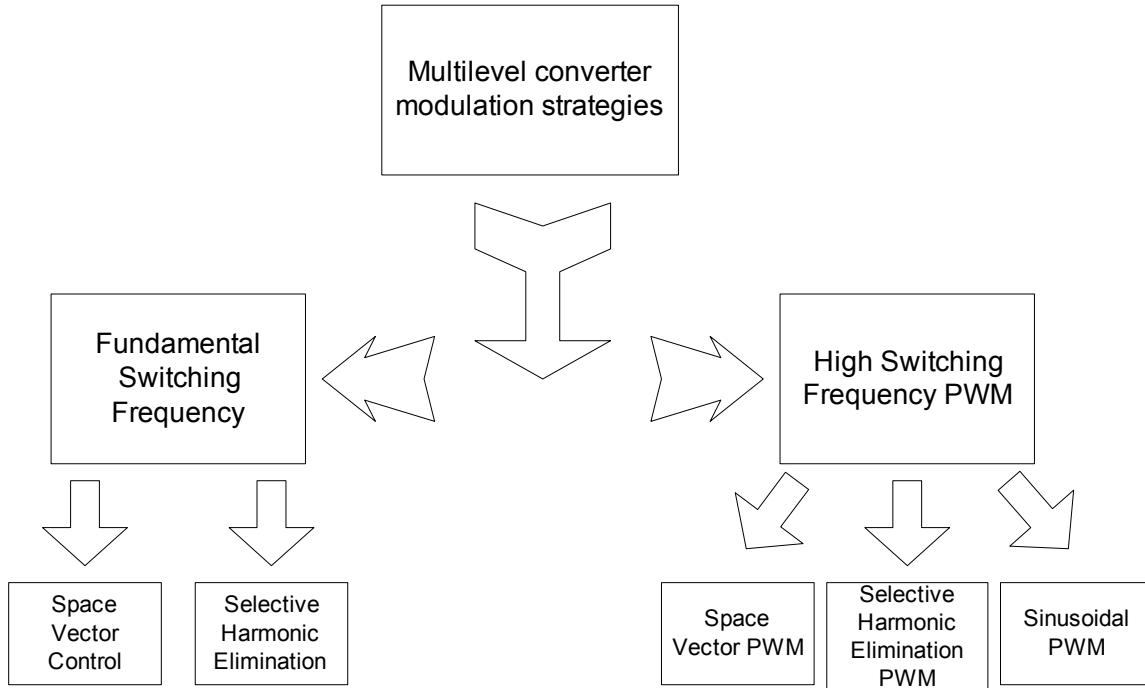
Pulse width modulation (PWM) strategies used in a conventional inverter can be modified to use in multilevel converters. The advent of the multilevel converter PWM modulation methodologies can be classified according to switching frequency as illustrated in Figure 31.13. The three multilevel PWM methods most discussed in the literature have been multilevel carrier-based PWM, selective harmonic elimination, and multilevel space vector PWM; all are extensions of traditional two-level PWM strategies to several levels. Other multilevel PWM methods have been used to a much lesser extent by researchers; therefore, only the three major techniques will be discussed in this chapter.



**Figure 31.11** Series-parallel connection to electrical system of two back-to-back inverters.



**Figure 31.12.** Six-level diode-clamped back-to-back converter structure.

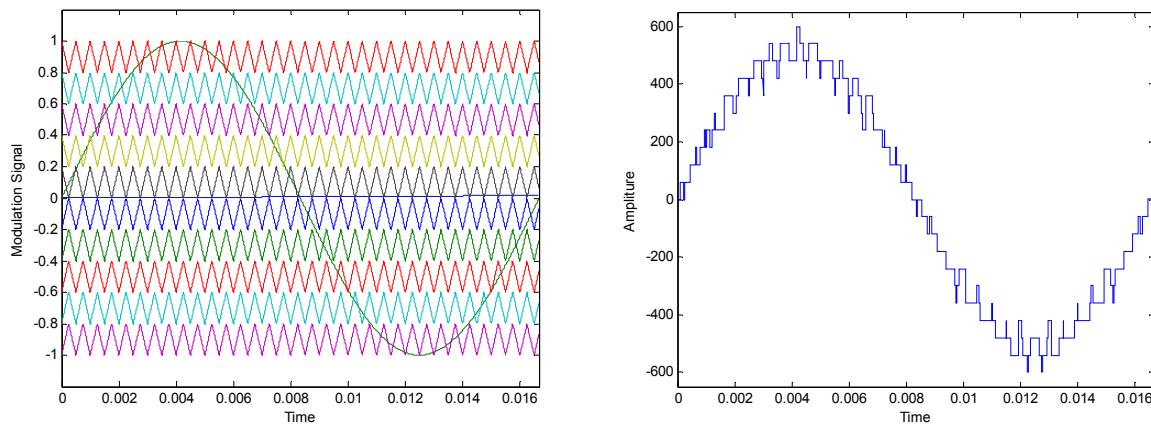


**Figure 31.13.** Classification of PWM multilevel converter modulation strategies.

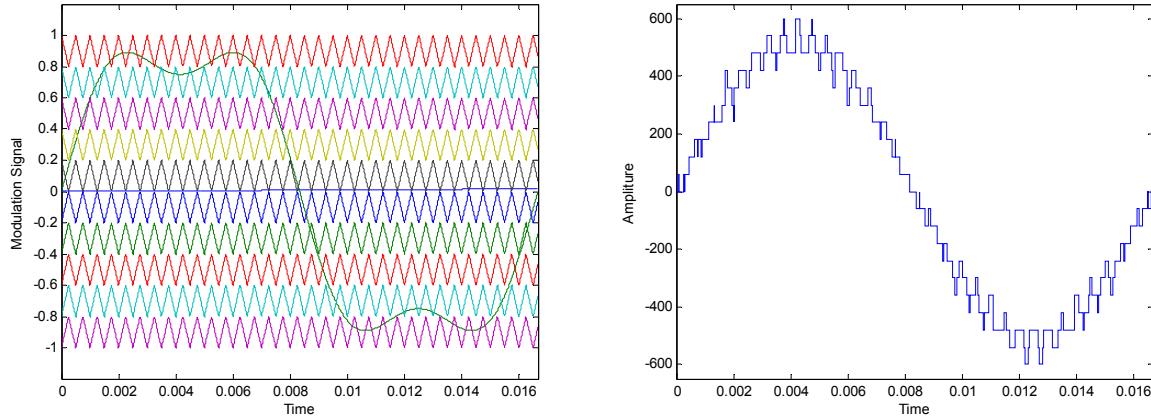
### 31.3.1 Multilevel carrier-based PWM

Several different two-level multilevel carrier-based PWM techniques have been extended by previous authors as a means for controlling the active devices in a multilevel converter. The most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase. Figure 31.14 illustrates three major carrier-based techniques used in a conventional inverter that can be applied in a multilevel inverter: sinusoidal PWM (SPWM), third harmonic injection PWM (THPWM), and space vector PWM (SVM). SPWM is a very popular method in industrial applications.

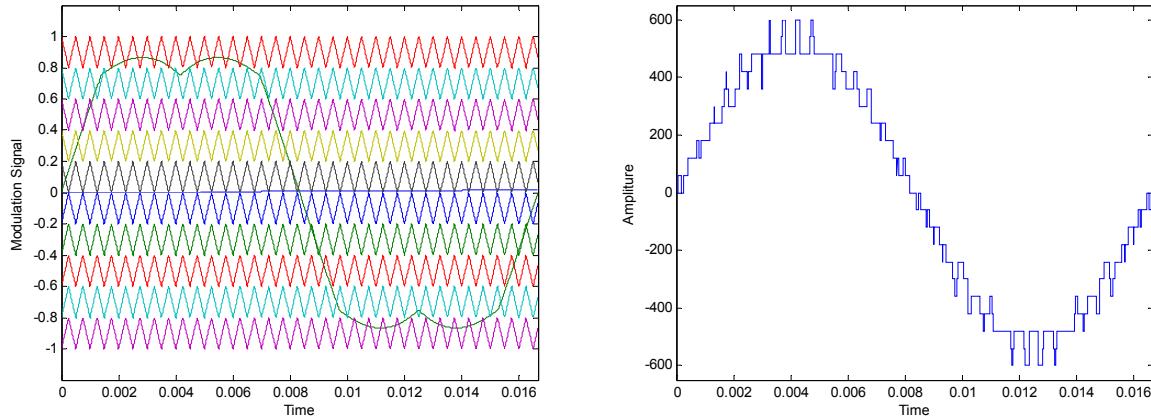
In order to achieve better dc link utilization at high modulation indices, the sinusoidal reference signal can be injected by a third harmonic with a magnitude equal to 25% of the fundamental; its line-line output voltage is shown in Figure 31.14(b). As can be seen in Figure 31.14 (b) and (c), the reference signals have some margin at unity amplitude modulation index. Obviously, the dc utilization of THPWM and SVM are better than SPWM in the linear modulation region. The dc utilization means the ratio of the output fundamental voltage to the dc link voltage. Other interesting carrier-based multilevel PWM are subharmonic PWM (SH-PWM) and switching frequency optimal PWM (SFO-PWM). In addition, some particular aspects of these carrier-based methods are also discussed as follows.



(a)



(b)



(c)

**Figure 31.14** Simulation of modulation signals and their line-line output voltage using five separate dc sources (60 volts each dc source) cascaded multilevel inverter with three major conventional carrier-based PWM techniques at unity modulation index and 2 kHz switching frequency. (a) SPWM, (b) THPWM, (c) SVM.

#### A. Subharmonic PWM

Carrara [49] extended SH-PWM to multiple levels as follows: For an  $m$ -level inverter,  $m-1$  carriers with the same frequency  $f_c$  and the same amplitude  $A_c$  are disposed such that the bands they occupy are contiguous. The reference waveform has peak-to-peak amplitude  $A_m$ , a frequency  $f_m$ , and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off.

In multilevel inverters, the amplitude modulation index,  $m_a$ , and the frequency ratio,  $m_f$ , are defined as

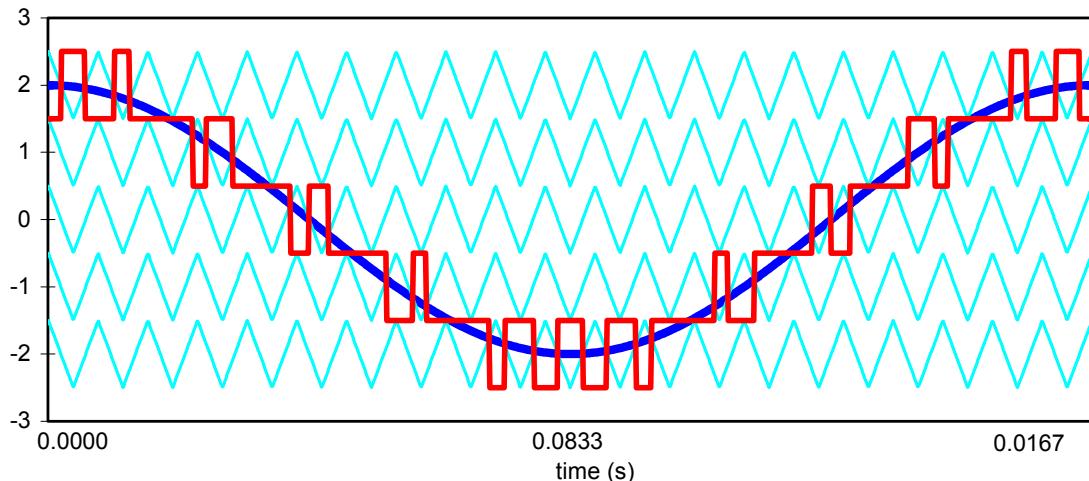
$$m_a = \frac{A_m}{(m-1) \cdot A_c}, \quad (31.3)$$

$$m_f = \frac{f_c}{f_m}. \quad (31.4)$$

Figure 31.15 shows a set of carriers ( $m_f = 21$ ) for a six-level diode-clamped inverter and a sinusoidal reference, or modulation, waveform with an amplitude modulation index of 0.8. The resulting output voltage of the inverter is also shown in Figure 31.15.

#### B. Switching Frequency Optimal PWM

Another carrier based method that was extended to multilevel applications by Menzies is termed switching frequency optimal PWM (SFO-PWM), and it is similar to SH-PWM except that a zero sequence (triplen harmonic) voltage is added to each of the carrier waveforms [50]. This method takes the instantaneous average of the maximum and minimum of the three reference voltages  $(V_a^*, V_b^*, V_c^*)$  and subtracts this value from each of the individual reference voltages, i.e.,



**Figure 31.15.** Multilevel carrier-based SH-PWM showing carrier bands, modulation waveform, and inverter output waveform ( $m = 6$ ,  $m_f = 21$ ,  $m_a = 0.8$ ).

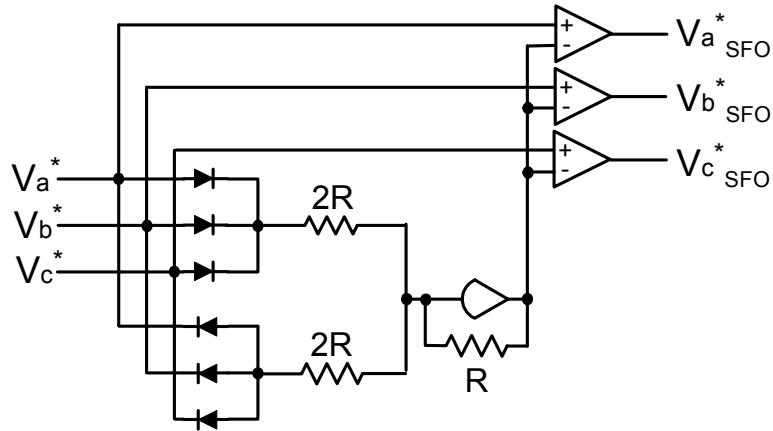
$$V_{offset} = \frac{\max(V_a^*, V_b^*, V_c^*) + \min(V_a^*, V_b^*, V_c^*)}{2}, \quad (31.5)$$

$$V_{aSFO}^* = V_a^* - V_{offset}, \quad (31.6)$$

$$V_{bSFO}^* = V_b^* - V_{offset}, \quad (31.7)$$

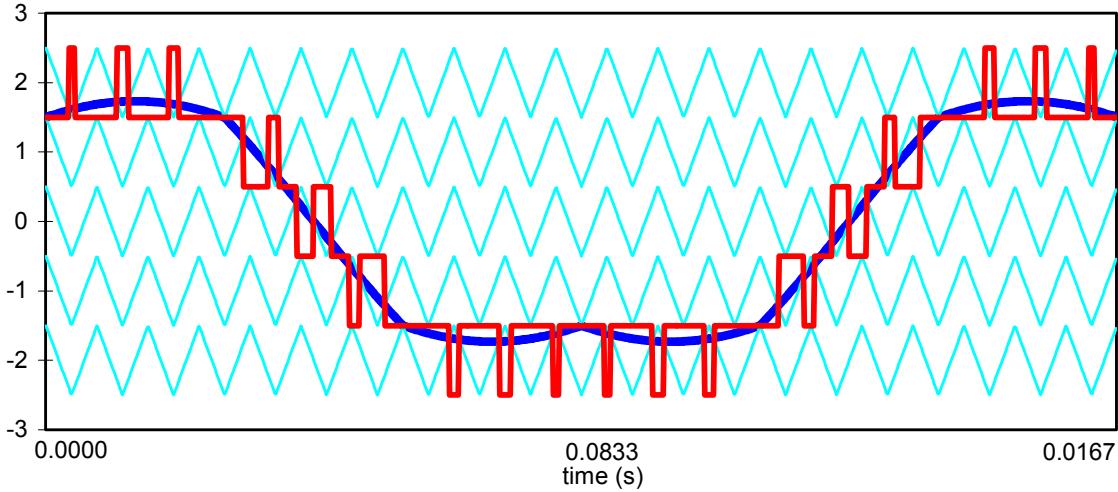
$$V_{cSFO}^* = V_c^* - V_{offset}. \quad (31.8)$$

The addition of this triplen offset voltage centers all of the three reference waveforms in the carrier band, which is equivalent to using space vector PWM [51, 52]. The analog equivalent of equations (31.5 through 31.8) is shown in Figure 31.16 [53]. SFO-PWM is illustrated in Figure 31.17 for the same reference voltage waveform that was used in Figure 31.15. The resulting output voltage of the inverter is also shown in Figure 31.17. The SFO-PWM technique enables the modulation index to be increased by 15 percent before the overmodulation region is reached.

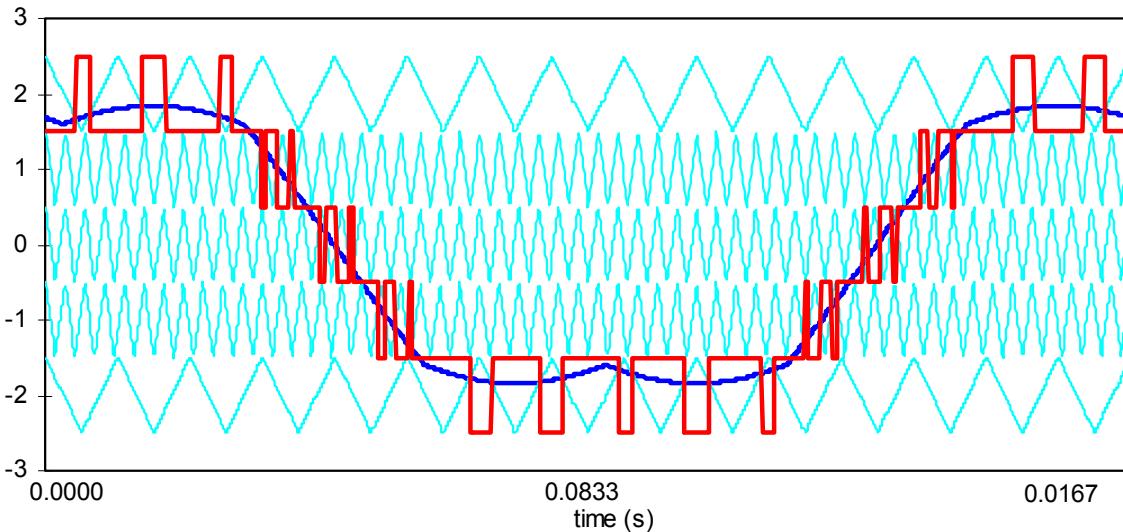


**Figure 31.16.** Analog circuit for zero sequence addition in SFO-PWM.

For the SH-PWM and SFO-PWM techniques shown in Figures 31.15 and 31.17, the top and bottom switches are switched much more often than the intermediate devices. Methods to balance and/or reduce the device switchings without an adverse affect on a multilevel inverter's output voltage total harmonic distortion would be beneficial. Methods to do just that are developed in [54]. A novel method to balance device switchings for all of the levels in a diode clamped inverter has been demonstrated for SH-PWM and SFO-PWM by varying the frequency for the different triangle wave carrier bands as shown in Figure 31.18 [54].



**Figure 31.17.** Multilevel carrier-based SFO-PWM showing carrier bands, modulation waveform, and inverter output waveform ( $m = 6$ ,  $m_f = 21$ ,  $m_a = 0.8$ ).



**Figure 31.18.** SFO-PWM where carriers have different frequencies ( $m_a = 0.85$ ,  $m_f = 15$  for Band<sub>2</sub>, Band<sub>-2</sub>;  $m_f = 55$  for Band<sub>1</sub>, Band<sub>-1</sub>, Band<sub>0</sub>,  $\varphi = 0.10$  rad).

### C. Modulation Index Effect on Level Utilization

For low amplitude modulation indices, a multilevel inverter will not make use of all of its levels and at very low modulation indices operate as if it is a traditional two-level inverter. Figure 31.19 shows two simulation results of what the output voltage waveform looks like at amplitude modulation indices of 0.5 and 0.15. Figure 31.19(a) shows how the bottom and top switches ( $S_{a1}-S_{a'1}$ ,  $S_{a5}-S_{a'5}$  in Figure 31.5) go unused for amplitude modulation indices less than 0.6 in a six-level inverter. Figure 31.19 (b) shows how only the middle switches ( $S_{a3}-S_{a'3}$  in Figure 31.5) change states when a six-level inverter is operated at an amplitude modulation index

less than 0.2. The output waveform in Figure 31.19(b) appears to be that of a traditional two-level inverter rather than a multilevel inverter.

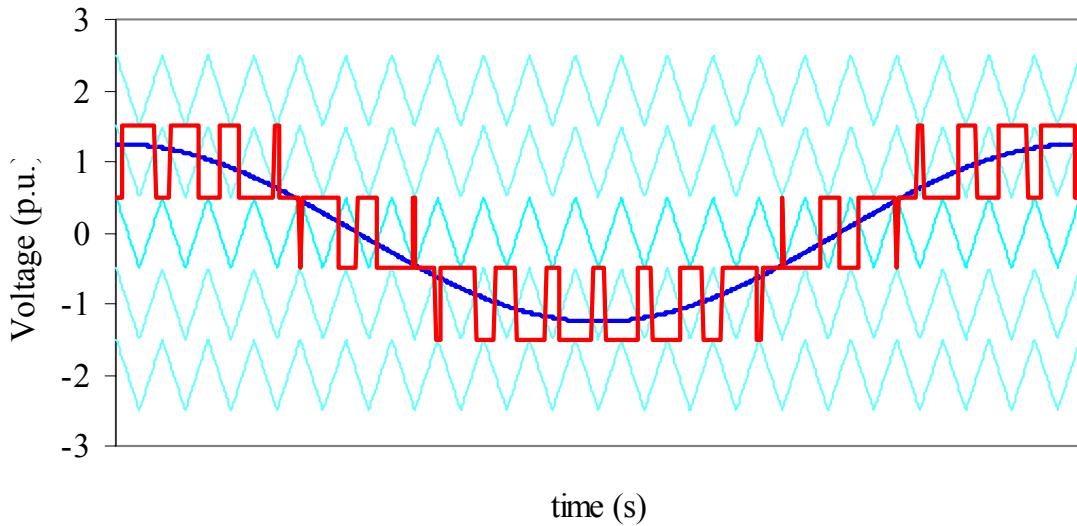
The minimum modulation index  $m_{a\min}$  for which a multilevel inverter controlled with SH-PWM makes use of all of its levels,  $m$ , is

$$m_{a\min} = \frac{m-3}{m-1}. \quad (31.9)$$

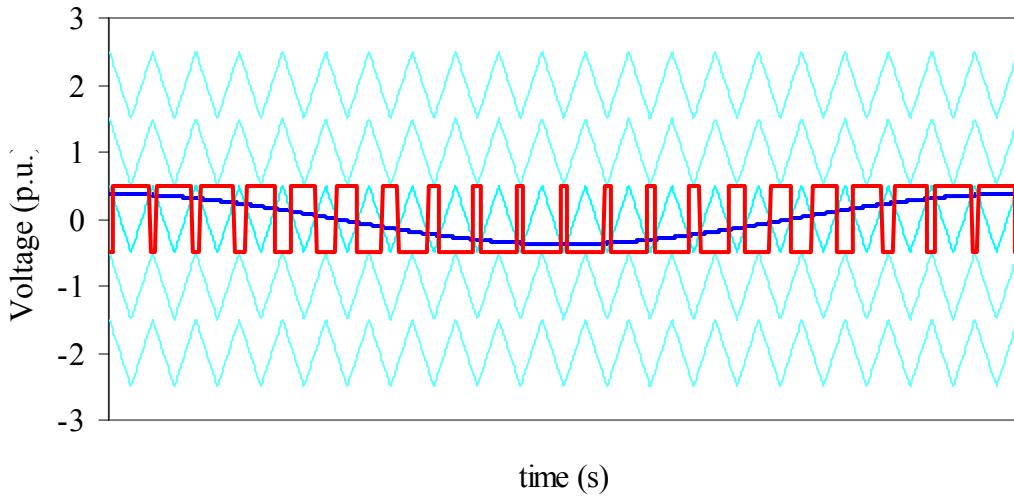
Table 31.3 lists the minimum modulation index where a multilevel inverter uses all its constituent levels for both SH-PWM and SFO-PWM techniques. Table 31.3 also shows that the maximum modulation index before pulse dropping (overmodulation) occurs is 1.000 for SH-PWM and 1.155 for SFO-PWM. As shown in Table 31.3, when a multilevel inverter operates at modulation indices much less than 1.000, not all of its levels are involved in the generation of the output voltage and simply remain in an unused state until the modulation index increases sufficiently. The table also shows that level usage is more likely to suffer to a greater extent as the number of levels in the inverter increases.

**Table 31.3.** Modulation index ranges without level reduction (Min) or pulse dropping because of overmodulation (Max).

Levels	SH-PWM		SFO-PWM	
	Min	Max	Min	Max
3	0.000	1.000	0.000	1.155
4	0.333	1.000	0.385	1.155
5	0.500	1.000	0.578	1.155
6	0.600	1.000	0.693	1.155
7	0.667	1.000	0.770	1.155
8	0.714	1.000	0.825	1.155
9	0.750	1.000	0.866	1.155
10	0.778	1.000	0.898	1.155
11	0.800	1.000	0.924	1.155
12	0.818	1.000	0.945	1.155
13	0.833	1.000	0.962	1.155



(a) SH-PWM,  $m = 6, m_a = 0.5$



(b) SH-PWM,  $m = 6, m_a = 0.15$

**Figure 31.19.** Level reduction in a six-level inverter at low modulation indices.

One way to make use of the multiple levels, even during low modulation periods, is to take advantage of the redundant output voltage states by rotating level usage in the inverter after each modulation cycle. This will reduce the switching stresses on some of the inner levels by making use of those outer voltage levels that otherwise would go unused.

As previously mentioned, diode-clamped inverters have redundant line-line voltage states for low modulation indices, but have no phase redundancies [55]. For an output voltage state  $(i, j, k)$  in an  $m$ -level diode-clamped inverter, the number of redundant states available is given by

$$N_{\substack{\text{redundancies} \\ \text{available}}} = m - 1 - [\max(i, j, k) - \min(i, j, k)]. \quad (31.10)$$

As the modulation index decreases, more redundant states are available. Table 31.4 shows the number of distinct and redundant line-line voltage states available in a six-level inverter for different output voltages.

In the next section, a carrier-based method is given that uses line-line redundancies in a diode-clamped inverter operating at a low modulation index so that active device usage is more balanced among the levels.

**Table 31.4.** Six-level inverter line-line voltage redundancies.

$\max(i, j, k) - \min(i, j, k)$	# Distinct States	# Redundancies per Distinct State	Total # of States
0	1	5	6
1	6	4	30
2	12	3	48
3	18	2	54
4	24	1	48
5	30	0	30
<i>Total</i>	91	---	216

#### D. Increasing Switching Frequency at Low Modulation Indices

For amplitude modulation indices less than 0.5, the level usage in odd-level inverters can be sufficiently rotated so that the switching frequency can be doubled and still keep the thermal losses within the limits of the device. For inverters with an even number of levels, the modulation index at which frequency doubling can be accomplished varies with the levels as shown in Table 31.5. This increase in switching frequency enables the inverter to compensate for higher frequency harmonics and will yield a waveform that more closely tracks a reference.

As an example of how to accomplish this doubling of inverter frequency, an analysis of a seven-level diode-clamped inverter with an amplitude modulation index of 0.4 is conducted. During one cycle, the reference waveform is centered in the upper three carrier bands; and during the next cycle, the reference waveform is centered in the lower three carrier bands as shown in Figure 31.20. This technique enables half of the switches to “rest” every other cycle and not incur any switching losses. With this method, the switching frequency (or carrier frequency  $f_c$  in the case of multilevel inverters) can effectively be doubled to  $2f_c$ , but the switches will have the same thermal losses as if they were switching at  $f_c$  but every cycle.

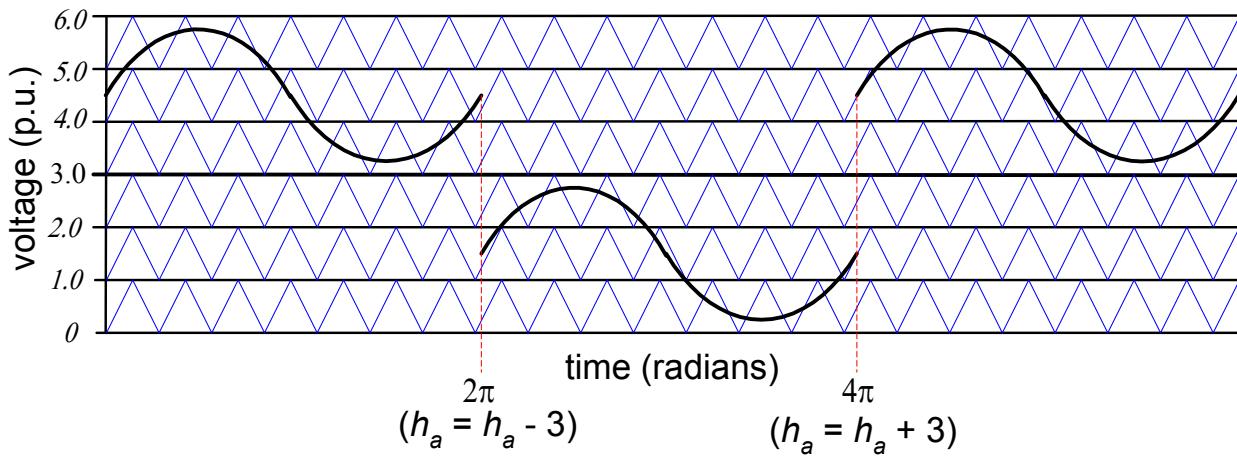
This method is possible only for three-wire systems because the diode-clamped inverter has line-line redundancies and no phase redundancies. This means that at the discontinuity where the reference moves from one carrier band set to another, the transition has to be synchronized such that all three phases are moved from one carrier set to the next set at the same time. In the case of frequency doubling, all three phases add or subtract the following number of states (or levels) every other reference cycle:

$$h_a(j+1) = h_a(j) + (-1)^j \cdot \frac{\lfloor \frac{m-1}{2} \rfloor}{2} \quad (31.11)$$

At modulation indices closer to zero, the switching frequency can be increased even more. This is possible because the reference waveform can be rotated among the carrier bands for a few cycles before returning to a previous set of switches for use. The switches are allowed to “rest” for a few cycles and thus are able to absorb higher losses during the cycle that they are in use. Table 31.5 shows the possible increased switching frequencies available at lower amplitude modulation indices for several different inverter levels.

Some additional switching loss is associated with the redundant switchings of the three phases at the end of each modulation cycle when rotating among carrier bands. For instance, for Figure 31.20 each of the three phases in the seven-level inverter will have three switch pairs change states at the end of every reference cycle. Compared to the switching loss associated with just the normal PWM switchings, however, this redundant switching loss is quite small, typically less than five percent of the total switching loss.

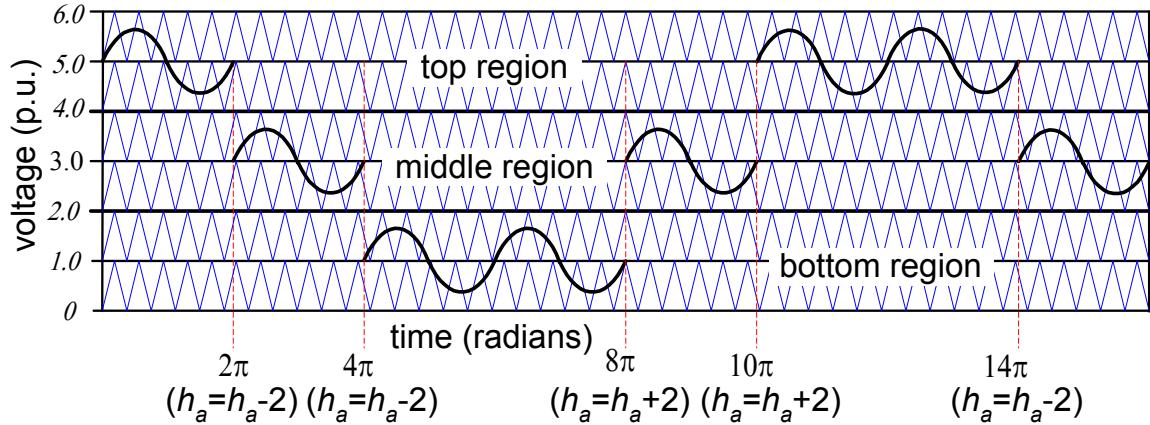
Figures 31.21 and 31.22 illustrate two different methods of rotating the reference waveform among three different regions (top, middle, and bottom) for modulation indices less than 0.333 in a seven-level inverter to enable the carrier frequency to be increased by a factor of three. The method shown in Figure 31.21 is preferred over that shown in Figure 31.22 because of less redundant state switching. The method in Figure 31.21 requires only four redundant state switchings every three reference cycles, whereas the method in Figure 31.22 requires eight redundant switchings every three reference cycles. In general for any multilevel inverter regardless of the number of levels or number of rotation regions, using the preferred reference rotation method will have  $\frac{1}{2}$  of the redundant switching losses that the alternate method would have.



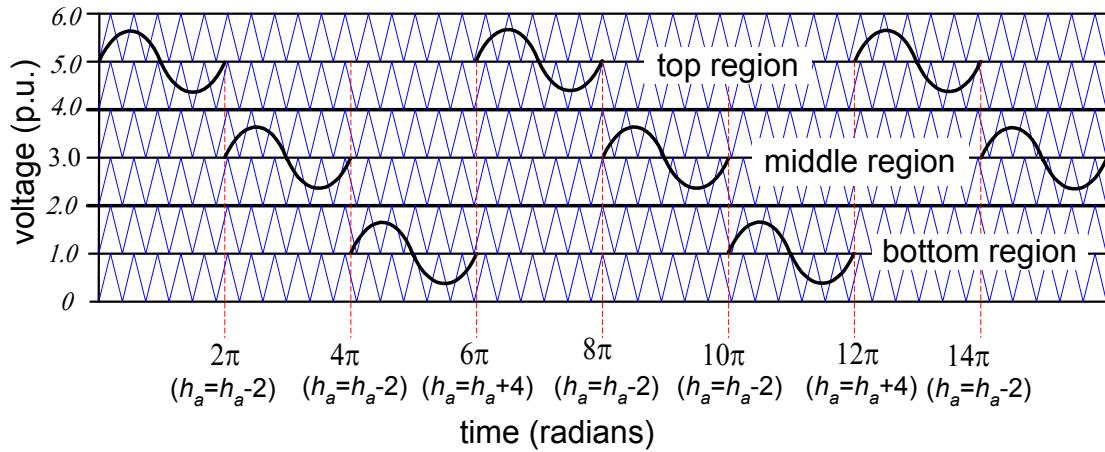
**Figure 31.20.** Reference rotation among carrier bands at low modulation indices ( $m_a < 0.5$ ).

**Table 31.5.** Increased switching frequency possible at lower modulation indices.

Inverter Levels	Modulation Index, $m_a$		Frequency Multiplier
	Min	Max	
3	0.000	0.500	2X
4	0.000	0.333	3X
5	0.250	0.500	2X
	0.000	0.250	4X
6	0.200	0.400	2X
	0.000	0.200	5X
7	0.333	0.500	2X
	0.167	0.333	3X
	0.000	0.167	6X
8	0.285	0.428	2X
	0.142	0.285	3X
	0.000	0.142	7X
9	0.25	0.500	2X
	0.125	0.250	4X
	0.000	0.125	8X
10	0.333	0.444	2X
	0.222	0.333	3X
	0.111	0.222	4X
	0.000	0.111	9X
11	0.333	0.500	2X
	0.200	0.333	3X
	0.000	0.200	5X
12	0.272	0.454	2X
	0.181	0.272	3X
	0.090	0.181	5X
	0.000	0.090	11X
13	0.333	0.500	2X
	0.250	0.333	3X
	0.167	0.250	4X
	0.0833	0.167	6X
	0.000	0.0833	12X



**Figure 31.21.** Preferred method of reference rotation among carrier bands with  $3\times$  carrier frequency at very low modulation indices.



**Figure 31.22.** Alternate method of reference rotation among carrier bands with  $3\times$  carrier frequency at very low modulation indices.

Unlike the diode-clamped inverter, the cascaded H-bridges inverter has phase redundancies in addition to the aforementioned line-line redundancies. Phase redundancies are much easier to exploit than line-line redundancies because the output voltage in each phase of a three-phase inverter can be generated independently of the other two phases when only phase redundancies are used. A method was given in [19] that makes use of these phase redundancies in a cascaded inverter so that each active device's duty cycle is balanced over  $(m-1)/2$  modulation waveform cycles regardless of the modulation index. The same pulse rotation technique used for fundamental frequency switching of cascade inverters was used but with a PWM output voltage waveform [56], which is a much more effective means of controlling a driven motor at low speeds than continuing to do fundamental frequency switching. The effect of this control is that the output waveform can have a high switching frequency but the individual levels can still switch at a constant switching frequency of 60 Hz if desired.

### 31.3.2 Multilevel space vector PWM

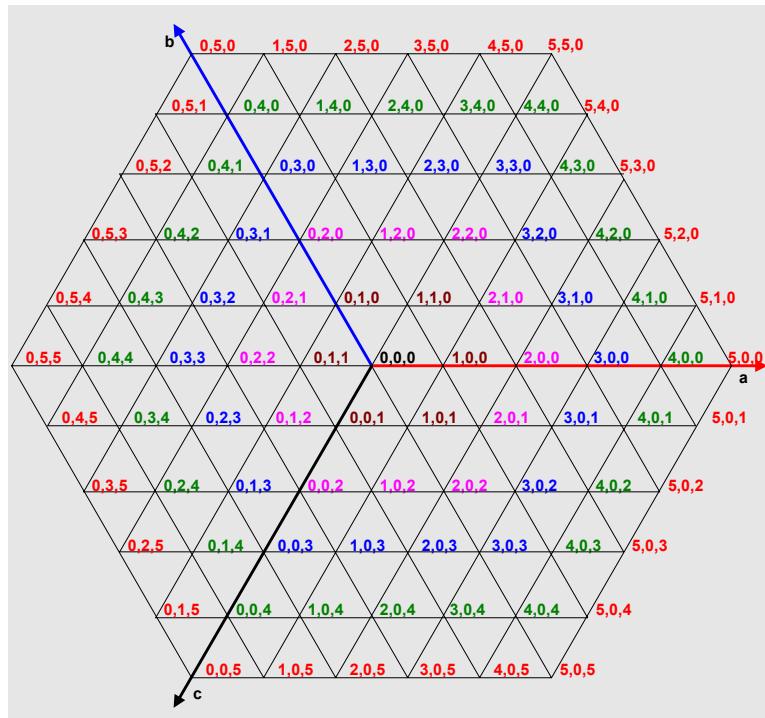
Choi [57] was the first author to extend the two-level space vector pulse width modulation technique to more than three levels for the diode-clamped inverter. Figure 31.23 shows what the space vector d-q plane looks like for a six-level inverter. Figure 31.24 represents the equivalent dc link of a six-level inverter as a multiplexer that connects each of the three output phase voltages to one of the dc link voltage tap points [58]. Each integral point on the space vector plane represents a particular three-phase output voltage state of the inverter. For instance, the point (3, 2, 0) on the space vector plane means, that with respect to ground, *a* phase is at  $3V_{dc}$ , *b* phase is at  $2V_{dc}$ , and *c* phase is at  $0V_{dc}$ . The corresponding connections between the dc link and the output lines for the six-level inverter are also shown in Figure 31.24 for the point (3, 2, 0). An algebraic way to represent the output voltages in terms of the switching states and dc link capacitors is described in the following [59]. For  $n = m-1$  where  $m$  is the number of levels in the inverter:

$$V_{abc0} = H_{abc}V_c, \quad (31.12)$$

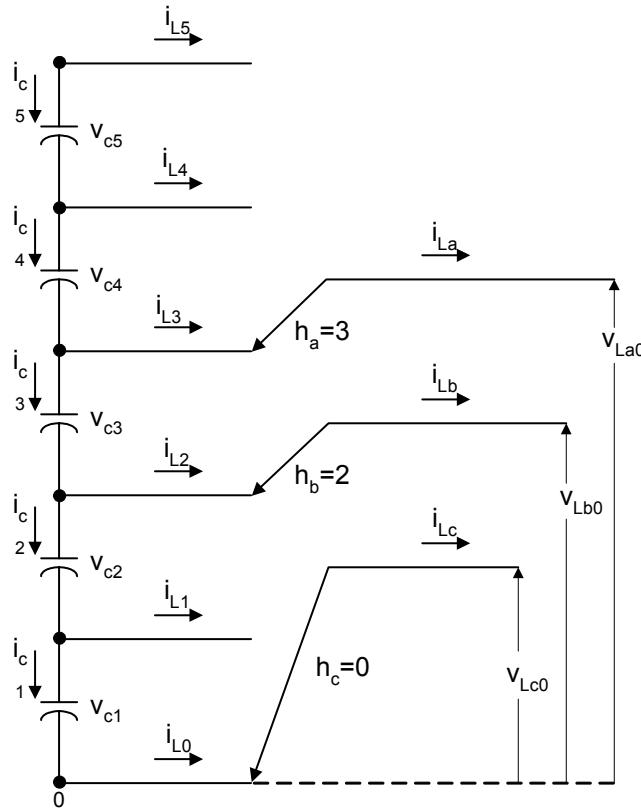
where  $V_c = [V_{c1} \ V_{c2} \ V_{c3} \ \dots \ V_{cn}]^T$ ,  $H_{abc} = \begin{bmatrix} h_{a1} & h_{a2} & h_{a3} & \dots & h_{an} \\ h_{b1} & h_{b2} & h_{b3} & \dots & h_{bn} \\ h_{c1} & h_{c2} & h_{c3} & \dots & h_{cn} \end{bmatrix}$ ,  $V_{abc0} = \begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix}$ , and

$$h_{aj} = \sum_j^n \delta(h_a - j),$$

where  $h_a$  is the switch state and  $j$  is an integer from 0 to  $n$ , and  
where  $\delta(x) = 1$  if  $x \geq 0$ ,  $\delta(x) = 0$  if  $x < 0$ .



**Figure 31.23.** Voltage space vectors for a six-level inverter.



**Figure 31.24.** Multiplexer model of diode-clamped six-level inverter.

Besides the output voltage state, the point (3, 2, 0) on the space vector plane can also represent the switching state of the converter. Each integer indicates how many upper switches in each phase leg are on for a diode-clamped converter. As an example, for  $h_a = 3$ ,  $h_b = 2$ ,  $h_c = 0$ , the  $H_{abc}$

matrix for this particular switching state of a six-level inverter would be  $H_{abc} = \begin{bmatrix} 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$ .

Redundant switching states are those states for which a particular output voltage can be generated by more than one switch combination. Redundant states are possible at lower modulation indices, or at any point other than those on the outermost hexagon shown in Figure 31.23. Switch state (3, 2, 0) has redundant states (4, 3, 1) and (5, 4, 2). Redundant switching states differ from each other by an identical integral value, i.e., (3, 2, 0) differs from (4, 3, 1) by (1, 1, 1) and from (5, 4, 2) by (2, 2, 2).

For an output voltage state  $(x, y, z)$  in an  $m$ -level diode-clamped inverter, the number of redundant states available is given by  $m - 1 - \max(x, y, z)$ . As the modulation index decreases (or the voltage vector in the space vector plane gets closer to the origin), more redundant states are available. The number of possible zero states is equal to the number of levels,  $m$ . For a six-level diode-clamped inverter, the zero voltage states are (0, 0, 0), (1, 1, 1), (2, 2, 2), (3, 3, 3), (4, 4, 4), and (5, 5, 5).

The number of possible switch combinations is equal to the cube of the level ( $m^3$ ). For this six-level inverter, there are 216 possible switching states. The number of distinct or unique states for an  $m$ -level inverter can be given by

$$m^3 - (m-1)^3 = \left[ 6 \sum_{n=1}^{m-1} n \right] + 1. \quad (31.13)$$

Therefore, the number of redundant switching states for an  $m$ -level inverter is  $(m-1)^3$ . Table 31.6 summarizes the available redundancies and distinct states for a six-level diode-clamped inverter.

**Table 31.6.** Line-line redundancies of six-level three-phase diode-clamped inverter.

Redundancies	Distinct States	Redundant States	Unique State Coordinates: (a, b, c) where $0 \leq a, b, c \leq 5$
5	1	5	(0,0,0)
4	6	24	(0,0,1), (0,1,0), (1,0,0), (1,0,1), (1,1,0), (0,0,1)
3	12	36	(p,0,2), (p,2,0), (0,p,2), (2,p,0), (0,2,p), (2,0,p) where $p \leq 2$
2	18	36	(0,3,p), (3,0,p), (p,3,0), (p,0,3), (3,p,0), (0,p,3) where $p \leq 3$
1	24	24	(0,4,p), (4,0,p), (p,4,0), (p,0,4), (4,p,0), (0,p,4) where $p \leq 4$
0	30	0	(0,5,p), (5,0,p), (p,5,0), (p,0,5), (5,p,0), (0,p,5) where $p \leq 5$
<i>Total</i>	<i>91</i>	<i>125</i>	<i>216 total states</i>

In two-level PWM, a reference voltage is tracked by selecting the two nearest voltage vectors and a zero vector and then by calculating the time required to be at each of these three vectors such that their sum equals the reference vector. In multilevel PWM, generally the nearest three triangle vertices,  $V_1$ ,  $V_2$ , and  $V_3$ , to a reference point  $V^*$  are selected so as to minimize the harmonic components of the output line-line voltage [60]. The respective time duration,  $T_1$ ,  $T_2$ , and  $T_3$ , required of these vectors is then solved from the following equations:

$$\vec{V}_1 T_1 + \vec{V}_2 T_2 + \vec{V}_3 T_3 = V^* T_s, \quad (31.14)$$

$$T_1 + T_2 + T_3 = T_s, \quad (31.15)$$

where  $T_s$  is the switching period. Equation (31.14) actually represents two equations, one with the real part of the terms and one with the imaginary part of the terms:

$$V_{1d} T_1 + V_{2d} T_2 + V_{3d} T_3 = V_d^* T_s, \quad (31.16)$$

$$V_{1q} T_1 + V_{2q} T_2 + V_{3q} T_3 = V_q^* T_s. \quad (31.17)$$

Equations (31.15) through (31.18) can then be solved for  $T_1$ ,  $T_2$ , and  $T_3$  as follows:

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \end{bmatrix} = \begin{bmatrix} V_{1d} & V_{2d} & V_{3d} \\ V_{1q} & V_{2q} & V_{3q} \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V_d^* T_s \\ V_q^* T_s \\ T_s \end{bmatrix}. \quad (31.18)$$

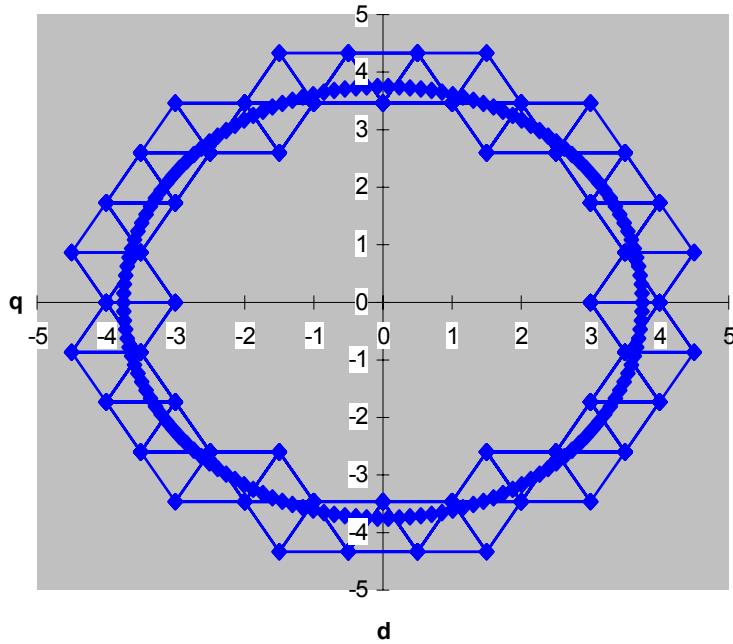
Others have proposed space vector methods that did not use the nearest three vectors, but these methods generally add complexity to the control algorithm. Figure 31.25 shows what a sinusoidal reference voltage (circle of points) and the inverter output voltages look like in the d-q plane.

Redundant switch levels can be used to help manage the charge on the dc link capacitors [62]. Generalizing from Figure 31.24, the equations for the currents through the dc link capacitors can be given as

$$i_{cn} = -i_{Ln}, \text{ and} \quad (31.19)$$

$$i_{c(n-j)} = -i_{L(n-j)} + i_{c(n-j+1)}, \text{ where } j = 1, 2, 3, \dots, n-1. \quad (31.20)$$

The dc link currents for  $h_a = 3, h_b = 2, h_c = 0$  would be  $i_{c5} = i_{c4} = 0, i_{c3} = -i_a, i_{c2} = -i_a - i_b, i_{c1} = -i_a - i_b$ . To see how redundant states affect the dc link currents, consider the two redundant states for (3, 2, 0). In state (4, 3, 1), the dc link currents would be  $i_{c5} = 0, i_{c4} = -i_a, i_{c3} = -i_a - i_b, i_{c2} = -i_a - i_b, i_{c1} = -i_a - i_b - i_c = 0$ ; and for the state (5, 4, 2), the dc link currents would be  $i_{c5} = -i_a, i_{c4} = -i_a - i_b, i_{c3} = -i_a - i_b, i_{c2} = i_{c1} = -i_a - i_b - i_c = 0$ .



**Figure 31.25.** Sinusoidal reference and inverter output voltage states in d-q plane.

From this example, one can see that the choice of redundant switching states can be used to determine which capacitors will be charged/discharged or unaffected during the switching period. While this control is helpful in balancing the individual dc voltages across the capacitors that make up the dc link, this method is quite complicated in selecting which of the redundant states to use. Constant use of redundant switching states also results in a higher switching frequency and lower efficiency of the inverter because of the extra switchings. Recently, optimized space vector switching sequences for multilevel inverters have been proposed in [63].

### 31.3.3 Selective Harmonic elimination

#### A. Fundamental switching frequency

The selective harmonic elimination method is also called fundamental switching frequency method based on the harmonic elimination theory proposed by Patel [64-65]. A typical 11-level multilevel converter output with fundamental frequency switching scheme is shown in Figure 31.2. The Fourier series expansion of the output voltage waveform as shown in Figure 31.2 is expressed in (31.1) and (31.2).

The conducting angles,  $\theta_1, \theta_2, \dots, \theta_s$ , can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [25].

For the 11-level case in Figure 31.2, the 5th, 7th, 11th, and 13th harmonics can be eliminated with the appropriate choice of the conducting angles. One degree of freedom is used so that the magnitude of the fundamental waveform corresponds to the reference waveform's amplitude or modulation index,  $m_a$ , which is defined as  $V_L^*/V_{Lmax}$ .  $V_L^*$  is the amplitude command of the inverter for a sine wave output phase voltage, and  $V_{Lmax}$  is the maximum attainable amplitude of the converter, i.e.,  $V_{Lmax} = s \cdot V_{dc}$ . The equations from (31.2) will now be as follows:

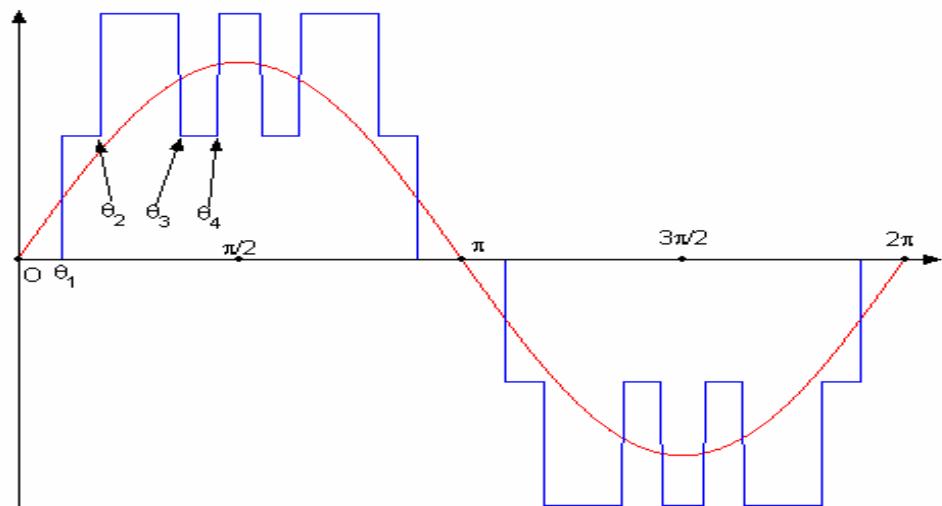
$$\begin{aligned} \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) &= 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) &= 0 \\ \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) &= 0 \\ \cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) &= 0 \\ \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) &= 5m_a \end{aligned} \quad (31.21)$$

These equations (31.21) are nonlinear transcendental equations that can be solved by an iterative method such as the Newton-Raphson method. For example, using a modulation index of 0.8 obtains:  $\theta_1 = 6.57^\circ, \theta_2 = 18.94^\circ, \theta_3 = 27.18^\circ, \theta_4 = 45.14^\circ, \theta_5 = 62.24^\circ$ . Thus, if the inverter output is symmetrically switched during the positive half cycle of the fundamental voltage to  $+V_{dc}$  at  $6.57^\circ$ ,  $+2V_{dc}$  at  $18.94^\circ$ ,  $+3V_{dc}$  at  $27.18^\circ$ ,  $+4V_{dc}$  at  $45.14^\circ$ , and  $+5V_{dc}$  at  $62.24^\circ$ , and similarly in the negative half cycle to  $-V_{dc}$  at  $186.57^\circ$ ,  $-2V_{dc}$  at  $198.94^\circ$ ,  $-3V_{dc}$  at  $207.18^\circ$ ,  $-4V_{dc}$  at  $225.14^\circ$ ,  $-5V_{dc}$  at  $242.24^\circ$ , the output voltage of the 11-level inverter will not contain the 5th, 7th, 11th, and 13th harmonic components [15,19]. Other methods to solve these equations include using genetic algorithms [68] and resultant theory [70-72].

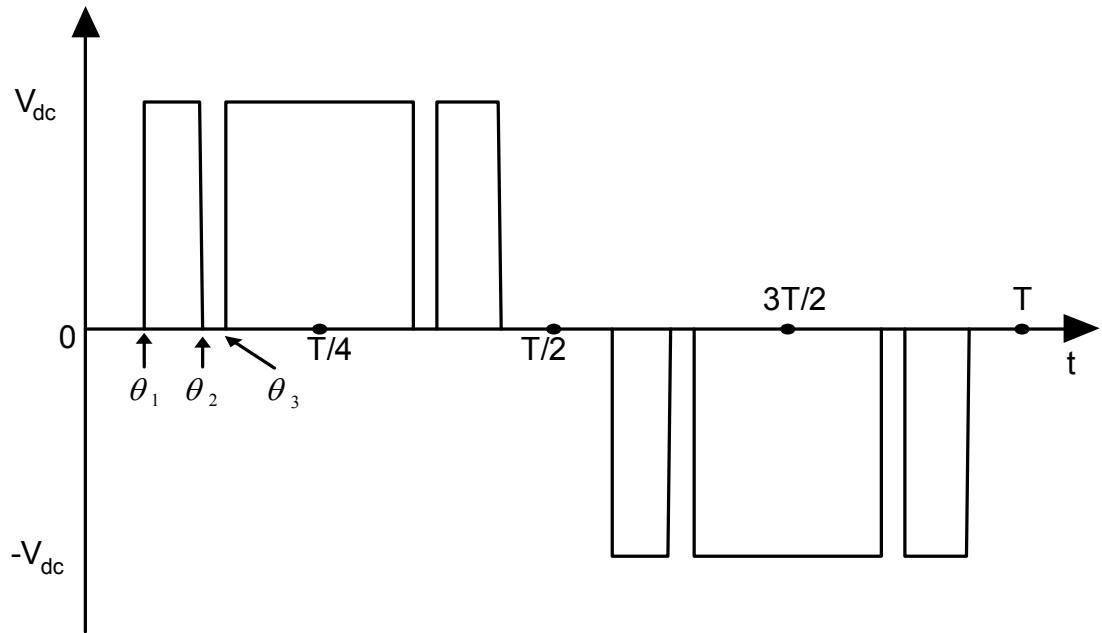
Practically, the precalculated switching angles are stored as the data in memory (look-up table). Therefore, a microcontroller could be used to generate the PWM gate drive signals.

#### B. Selective harmonic elimination PWM

In order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveforms, a generalized selective harmonic modulation method [66-67] was proposed, which is called virtual stage PWM [68]. An output waveform is shown in Figure 31.26. The Virtual Stage PWM is a combination of Unipolar Programmed PWM and the fundamental frequency switching scheme. The output waveform of Unipolar Programmed PWM is shown in Figure 31.27. When Unipolar Programmed PWM is employed on a multilevel converter, typically one DC voltage is involved, where the switches connected to the DC voltage are switched “on” and “off” several times per fundamental cycle. The switching pattern decides what the output voltage waveform looks like.



**Figure 31.26.** Output waveform of virtual stage PWM control.



**Figure 31.27.** Unipolar switching output waveform.

For fundamental switching frequency method, the number of switching angles is equal to the number of DC sources. However, for the Virtual Stage PWM method, the number of switching angles is not equal to the number of DC voltages. For example, in Figure 31.26, only two DC voltages are used, whereas there are four switching angles.

Bipolar Programmed PWM and Unipolar Programmed PWM could be used for modulation indices too low for the applicability of the multilevel fundamental frequency switching method. Virtual Stage PWM can also be used for low modulation indices. Virtual Stage PWM will produce output waveforms with a lower THD most of the time [68]. Therefore, Virtual Stage PWM provides another alternative to Bipolar Programmed PWM and Unipolar Programmed PWM for low modulation index control.

The major difficulty for selective harmonic elimination methods, including the fundamental switching frequency method and the Virtual Stage PWM method, is to solve the transcendental equations 31.21 for switching angles. Newton's method can be used to solve equations 31.21, but it needs good initial guesses, and solutions are not guaranteed. Therefore, Newton's method is not feasible to solving equations for large number of switching angles if good initial guesses are not available [69].

Recently, the resultant method has been proposed in [70-72] to solve the transcendental equations for switching angles. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Elimination resultant theory has been employed to determine the switching angles to eliminate specific harmonics, such as the 5<sup>th</sup>, 7<sup>th</sup>, 11<sup>th</sup>, and the 13<sup>th</sup>. However, as the number of DC voltages or the number of switching angles increases, the degrees of the polynomials in these equations become bulky. To conquer this problem, the fundamental frequency switching angle computation is solved by Newton's method. The initial guess can be provided by the results of lower order transcendental equations by the resultant method [69].

## 31.4 Multilevel converter design example

The objective of this section is to give a general idea how to design a multilevel converter in a specific application. Different applications for multilevel converters might have different specification requirements. Therefore, the multilevel universal power conditioner (MUPC) is utilized to demonstrate as the design example in this section.

Multilevel diode clamped converters can be designed where different levels have unequal voltage and current ratings; however, this approach would lose the advantage of being able to use identical, modular units for each leg of the inverter. The method used in this chapter to specify a back-to-back diode clamped converter for use as a universal power conditioner is for all voltage levels and legs in each of the two inverters to be the same. (The current ratings in the series inverter may be different than those in the parallel inverter.) This approach also allows the control system to extend the frequency range of the inverter by exploiting the additional voltage redundancies available at lower modulation indices as discussed in [73].

### 31.4.1 Interface with electrical system

Figure 31.28 illustrates the proposed electrical system connection topology for two diode-clamped inverters connected back-to-back and sharing a common dc bus. One inverter interfaces with the electrical system by means of a parallel connection through output inductors  $L_{PI}$ . The other inverter interfaces with the electrical system through a set of single-phase transformers in a series fashion. The primaries of the transformers are inserted in series with each of the three phase conductors supplied from a utility. The secondaries of the transformers are connected in an ungrounded wye and to the output of the series inverter. By having two inverters, this arrangement allows both the source voltage and the load current to be compensated

independently of each other [73-74]. With only a single inverter, regulating the load voltage and source current at the same time would not be possible.

The voltage injected into the electrical system by the series inverter compensates for deviations in the source voltage such that a regulated distortion-free waveform is supplied to the load. The parallel inverter injects current into the electrical system to compensate for current harmonics and/or reactive current demanded by the load such that the current drawn from the utility is in phase with the source voltage and contains no harmonic components.

### 31.4.2 Number of levels and voltage rating of active devices

In a multilevel inverter, determining the number of levels will be one of the most important factors because this affects many of the other sizing factors and control techniques. Tradeoffs in specifying the number of levels that the power conditioner will need and the advantages and complexity of having multiple voltage levels available are the primary differences that set a multilevel filter apart from a single level filter.

As a starting point, known is the nominal RMS voltage rating,  $V_{nom}$ , of the electrical system to which the diode clamped power conditioner will be connected. The dc link voltage must be at least as high as the amplitude of the nominal line-neutral voltage at the point of connection, or  $\sqrt{2} \cdot V_{nom}$ .

The parallel inverter must be able to inject currents by imposing a voltage across the parallel inductors,  $L_{PI}$ , that is the difference between the load voltage  $V_L$  and parallel inverter output voltage  $V_{PI}$ . The most difficult time to impose a voltage across the inductors is when the load voltage waveform is at its maximum or minimum. Simulation results have shown that the amplitude of the desired load voltage  $V_{nom}$  should not be more than 70 percent of the overall dc link voltage for the parallel inverter to have sufficient margin to inject appropriate compensation currents. Without this margin, complete compensation of reactive currents may not be possible. This margin can be incorporated into a design factor for the inverter. Because the dc link voltage and the voltage at the connection point can both vary, the design factor used in the rating selection process incorporates these elements as well as the small voltage drops that occur in the inverters during active device conduction.

The product of the number of the active devices in series ( $m-1$ ) and the voltage rating of the devices  $V_{dev}$  must then be such that

$$V_{device \ rating} \cdot (m-1) \geq \sqrt{2} \cdot V_{nom} \cdot D_{design \ factor} \quad (31.22)$$

The minimum number of levels and the voltage rating of the active devices (IGBTs, GTOs, power MOSFETs, etc.) are inversely related to each other. More levels in the inverter will lower the required voltage device rating of individual devices; or looking at it another way, a higher voltage rating of the devices will enable a fewer minimum number of levels to be used.

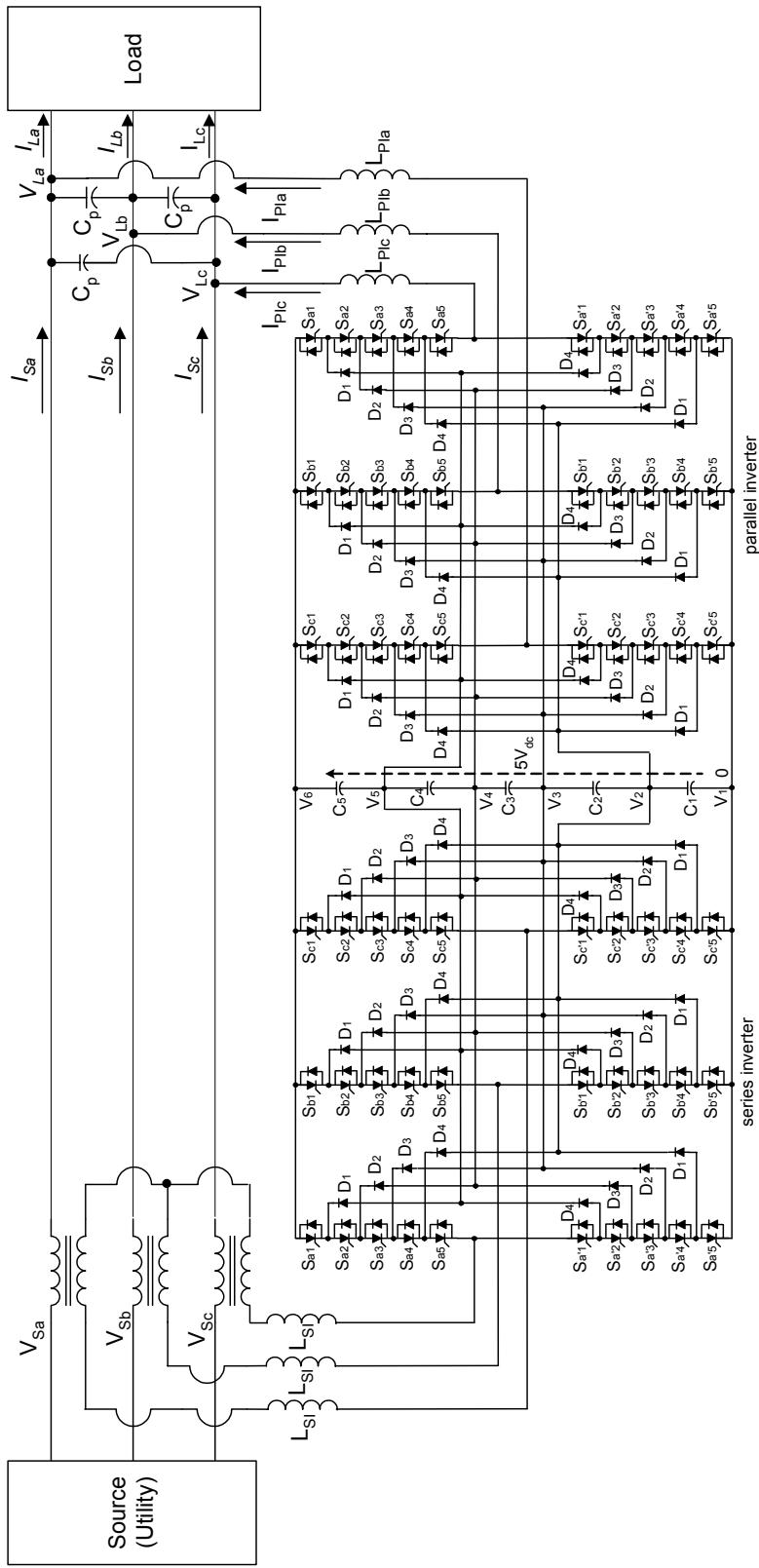


Figure 31.28. Electrical system connection of multilevel diode-clamped power conditioner.

Increasing the number of levels does not affect the total voltage blocking capability of the active devices in each phase leg because lower device ratings can be used. Some of the benefits of using more than the minimum required number of levels in a diode clamped inverter are as follows:

1. Voltage stress across each device is lower. Both active devices and dc link capacitors could be used that have lower voltage ratings (which sometimes are much cheaper and have greater availability).
2. The inverter will have a lower EMI because the  $dV/dt$  during each switching will be lower.
3. The output of the waveform will have more steps, or degrees of freedom, which enables the output waveform to more closely track a reference waveform.
4. Lower individual device switching frequency will achieve the same results as an inverter with a fewer number of levels and higher device switching frequency. Or the switching frequency can be kept the same as that in an inverter with a fewer number of levels to achieve a better waveform.

The drawbacks of using more than the required minimum number of levels are as follows:

1. Six active device control signals (one for each phase of the parallel inverter and the series inverter) are needed for each hardware level of the inverter – i.e.,  $6 \cdot (m-1)$  control signals. Additional levels require more computational resources and add complexity to the control.
2. If the blocking diodes used in the inverter have the same rating as the active devices, their number increases dramatically because  $6 \cdot (m-2) \cdot (m-1)$  diodes would be required for the back-to-back structure.

Considering the trade-offs between the number of levels and the voltage rating of the devices will generally lead the designer to choose an appropriate value for each.

### 31.4.3 Number and voltage rating of clamping diodes

As shown in the previous section,  $6 \cdot (m-1) \cdot (m-2)$  clamping diodes are required for an  $m$ -level back-to-back converter if the diodes have the same voltage rating as the active devices. As discussed in section 31.2, the voltage rating of each series of clamping diodes is designated by the subscript of the diode shown in Figure 31.28. For instance,  $D_4$  must block  $4V_{dc}$ ,  $D_3$  must block  $3V_{dc}$ , and so on.

If diodes that have higher voltage ratings than the active devices are available, then the number of diodes required can be reduced accordingly. When considering diodes of different ratings, the minimum number of clamping diodes per phase leg of the inverter is  $2 \cdot (m-2)$  and for the complete back-to-back converter,  $12 \cdot (m-2)$ . Unlike the active devices, additional levels do *not* enable a decrease in the voltage rating of the clamping diodes. In each phase leg, note that the voltage rating of each pair of diodes adds up to the overall dc link voltage  $(m-1) \cdot V_{dc}$ . Considering the six-level converter in Figure 31.28, connected to voltage level  $V_5$  are the anode of  $D_1$  and the cathode of  $D_4$ .  $D_1$  must be able to block  $V_{dc}$ , and  $D_4$  must block  $4V_{dc}$ ; the sum of their voltage blocking capabilities is  $5V_{dc}$ . For voltage level  $V_4$ , the anode of  $D_2$  and the cathode

of  $D_3$  are connected together to this point. Again, the sum of their voltage blocking capability is  $2V_{dc} + 3V_{dc} = 5V_{dc}$ . The same is true for the other intermediate voltage levels. Therefore, the total voltage blocking capability per phase of an  $m$ -level converter is  $(m-2) \cdot (m-1) \cdot V_{dc}$  and for the back-to-back converter,

$$V_{clamp_{total}} = 6 \cdot (m-2) \cdot (m-1) \cdot V_{dc}. \quad (31.23)$$

Each additional level added to the converter will require an additional  $6 \cdot (m-1) \cdot V_{dc}$  in voltage blocking capabilities. From this, one can see that unnecessarily adding more than the required number of voltage levels can quickly become cost prohibitive.

### 31.4.4 Current rating of active devices

In order to determine the required current rating of the active switching devices for the parallel and series portions of the back-to-back converter shown in Figure 31.28, the maximum apparent power that each inverter will either supply or draw from the electrical system must be known. These ratings will largely depend on the compensation objectives and to what limits they are specified to maintain. Of the three voltage compensation objectives (voltage sag, unbalanced voltages, voltage harmonics), the greatest power demands of the series inverter will almost always occur during voltage sag conditions. For the parallel inverter, generally the reactive power compensation demands will dominate the design of the converter, as opposed to harmonic current compensation.

For this analysis, balanced voltage sag conditions will be considered in the specification of the power ratings of the two inverters. A one-line diagram circuit is shown in Figure 31.29 for the converter and electrical system represented in Figure 31.28. Equations can be developed for the apparent power required of each of the inverters based on the three phase rated apparent load power  $S_{Lnom}$ , rated line-line load voltage  $V_{Lnom}$ , and line-line source voltage  $V_S$  [75].

#### A. Series inverter power rating

First, the rating of the series inverter will be considered. The voltage  $V_{SI}$  across the series transformer shown in Figure 31.29, is given by the vector equation:

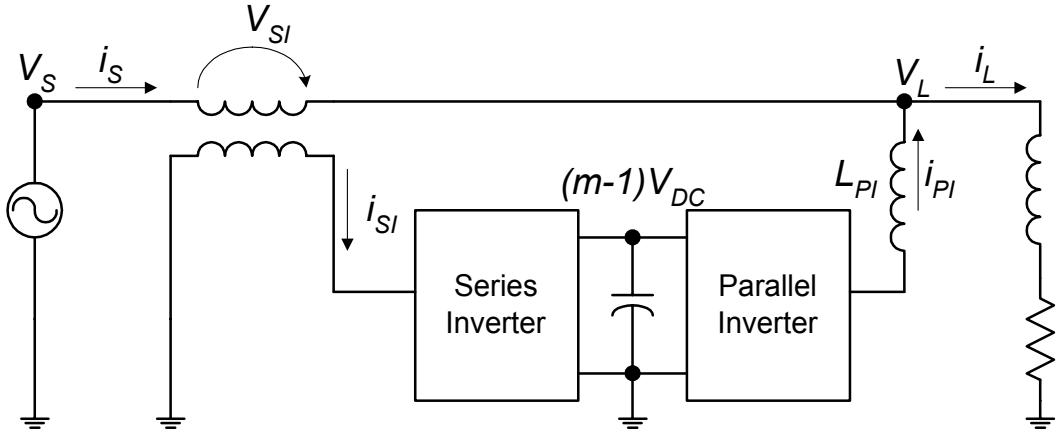
$$\bar{V}_{SI} = \bar{V}_L - \bar{V}_S. \quad (31.24)$$

The apparent power delivered from the series converter can then be given as

$$\bar{S}_{SI} = (\bar{V}_L - \bar{V}_S) \cdot \bar{I}_S^*. \quad (31.25)$$

If the load voltage  $V_L$  is regulated such that it is in phase with the source voltage  $V_S$ , then (31.24) can be rewritten as an algebraic equation:

$$V_{SI} = V_L - V_S. \quad (31.26)$$



**Figure 31.29.** One line diagram of a MUPC connected to the electrical system.

Assuming that the back-to-back converter is lossless, the entire real power  $P_L$  drawn by the load must be supplied by the utility source,  $P_S = P_L$ . If the source current is regulated such that it is in phase with the source voltage, then

$$P_S = V_S \cdot I_S = P_L. \quad (31.27)$$

Combining (31.25) through (31.27), the real power delivered from the series converter is

$$P_{SI} = (V_L - V_S) \cdot I_S. \quad (31.28)$$

Multiplying and dividing the right side of (31.28) by  $V_s$  yields

$$P_{SI} = \left( \frac{V_L}{V_S} - \frac{V_S}{V_S} \right) \cdot I_S \cdot V_S. \quad (31.29)$$

Substituting (31.27) into (31.29) produces the following equation for the rated apparent power of the series inverter:

$$S_{SI} = P_{SI} = P_L \cdot \left( \frac{V_L}{V_S} - 1 \right). \quad (31.30)$$

Choosing the rated load power  $S_L$  and the rated load voltage  $V_L$  as bases, Figure 31.30 shows the apparent power  $S_{SI}$  in per unit that the series inverter must provide as a function of the source voltage  $V_S$ . Each of the curves in Figure 31.30 is for loads of different power factors. As shown in Figure 31.30, the apparent power that the series inverter has to transfer is proportional to the power factor of the load [75].

Figure 31.30(a) shows that for voltage sags less than 50% of nominal, the series inverter would have to be rated to transfer more power than the rated load power, which in most applications would not be practical. Figure 31.30 (b) shows that for sags that are small in

magnitude, the series inverter would have a rating much less than that of the rated load power. For example, for a 20% voltage sag ( $V_s = 0.8 \cdot V_{nom}$ ), the required power rating of the series inverter is only 25% of the rated load.

When considering selection of the active devices for the series inverter, as shown in Figure 31.30, the magnitude of the voltage sag to be compensated will play a large role in determining the current rating required. The formula for determining the current rating of each of the devices as a function of the minimum source voltage to be compensated,  $\min(V_s)$ , is given in (31.31):

$$I_{\substack{SI \\ device \\ rating}} = \frac{S_{Lnom} \cdot \left( \frac{V_{nom}}{V_{nom} - \min(V_s)} - 1 \right)}{\sqrt{3} \cdot V_{nom}} \cdot D_{\substack{safety \\ factor}} . \quad (31.31)$$

The safety factor, or design factor, in (31.31) should be chosen to allow for future growth in the load supplied by the utility and compensated by the power conditioner.

### B. Parallel Inverter Power Rating

The power rating of the parallel inverter will now be considered. From Figure 31.29, the apparent power delivered to the electrical system by the parallel inverter can be expressed as

$$\bar{S}_{PI} = \bar{S}_L - \bar{V}_L \cdot \bar{I}_S^* = (P_L + jQ_L) - V_L I_S , \quad (31.32)$$

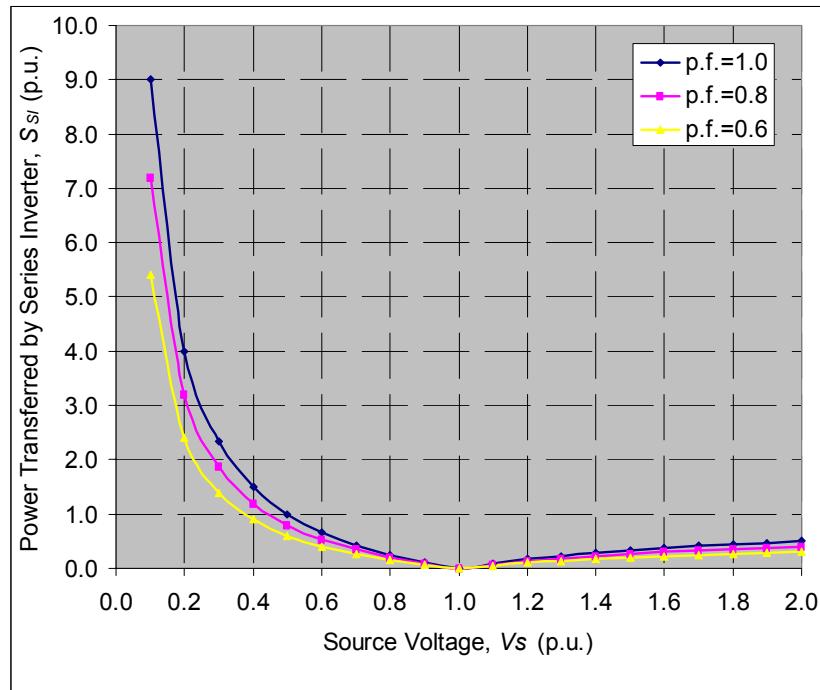
because the source current  $I_s$  and load voltage  $V_L$  are controlled such that they are in phase with the source voltage [75]. Multiplying and dividing the second term of (31.32) by  $V_S$  and substituting equation (31.27) yields the following:

$$V_L \cdot I_S = \frac{V_L}{V_S} \cdot V_S I_S = \frac{V_L}{V_S} \cdot P_L . \quad (31.33)$$

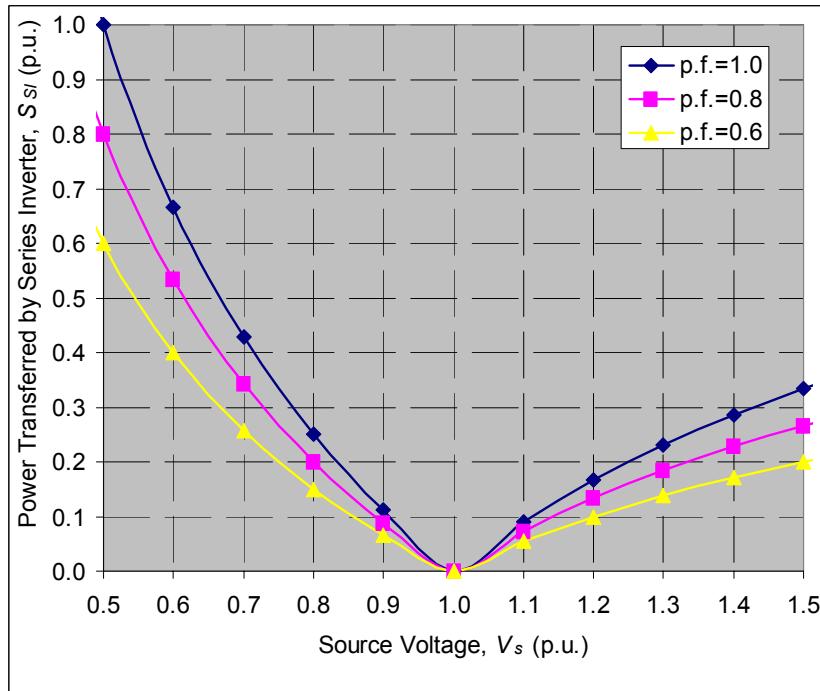
Substituting (31.33) into (31.32) and combining like terms yields

$$\bar{S}_{PI} = P_L \cdot \left( 1 - \frac{V_L}{V_S} \right) + jQ_L . \quad (31.34)$$

Figure 31.31 shows the apparent power  $S_{PI}$  in per unit that the parallel inverter must provide as a function of the source voltage  $V_S$  for loads of different power factors. Because the power transferred for voltage dips to less than 50% of nominal is predominantly real power, the parallel inverter would have to have an extraordinarily high rating if the conditioner were designed to compensate for such large voltage sags, just like the series inverter. From Figure 31.31(b), one can see that for a voltage sag to 50% of nominal, the parallel inverter has to draw a current  $I_{PI}$  equal to that drawn by the rated load,  $I_L$ . Unlike the series inverter, however, the dominant factor in determining the power rating of the parallel inverter is the load power factor if the conditioner is designed to compensate for only marginal voltage sags as shown in Figure 31.31(b).

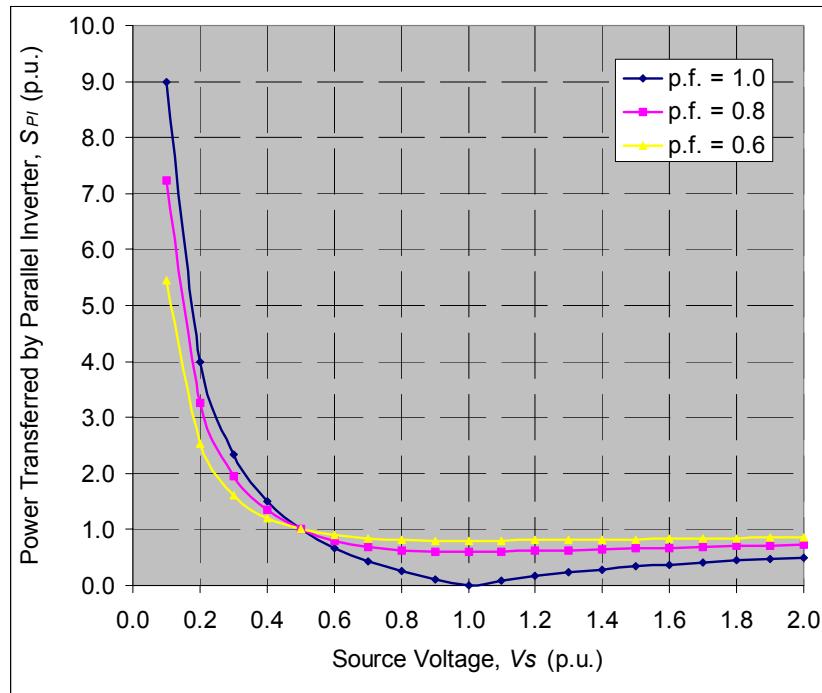


(a)

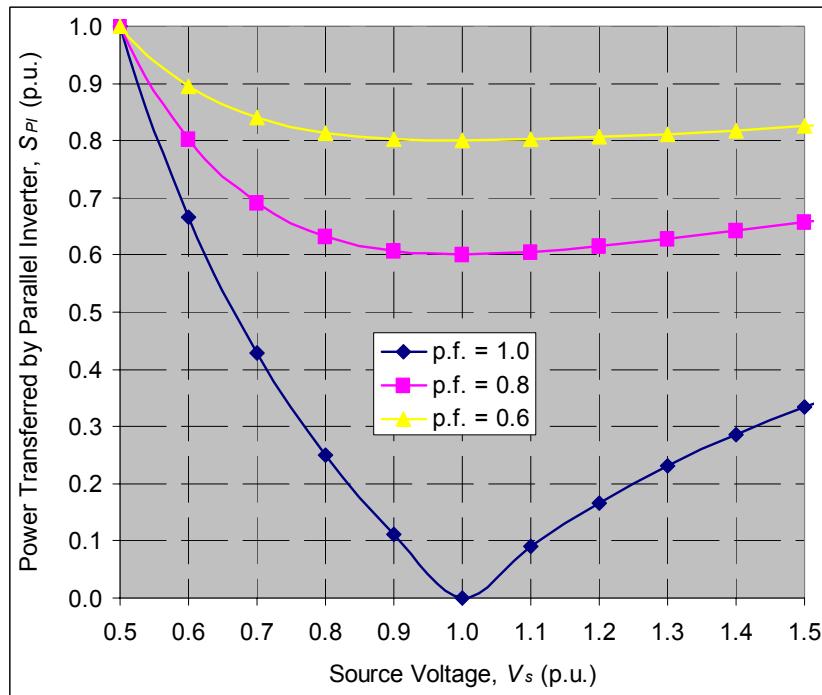


(b)

**Figure 31.30.** Apparent power requirements of series inverter during voltage sags.



(a)



(b)

**Figure 31.31.** Apparent power requirements of parallel inverter during voltage sags.

If the design of the universal power conditioner is to compensate for voltage sags to less than 50% of nominal voltage, then equation (31.31) should be used to determine the current rating of the parallel inverter. If the design of the conditioner is for marginal voltage sags (to 70% of nominal voltage) and the MUPC will be applied to a customer load that has a power factor of less than 0.9, then the following equation is more suited for calculating the current rating of the parallel inverter's active devices:

$$I_{PI_{device rating}} = \frac{Q_{Lnom}}{\sqrt{3} \cdot V_{nom}} \cdot D_{design factor} = \frac{S_{Lnom} \cdot (1 - (p.f.)^2)^{1/2}}{\sqrt{3} \cdot V_{nom}} \cdot D_{design factor}. \quad (31.35)$$

One common design for the parallel inverter in a universal power conditioner is for the inverter to have a current rating equal to that of the rated load current  $I_L$ .

### 31.4.5 Current rating of clamping diodes

When a multilevel inverter outputs an intermediate voltage level, not 0 or  $(m-1) \cdot V_{dc}$ , only one clamping diode in each phase leg conducts current at any instant in time whereas half of the active switches are conducting at all times. Which diode is conducting current is determined by which intermediate dc voltage level is connected to the output phase conductor and by which direction the current is flowing, positive or negative. For instance, when a phase leg of the series inverter in Figure 31.28 is connected to level  $V_4$ , then diode  $D_2$  conducts for current flowing from the inverter to the electrical system, and diode  $D_3$  conducts for current flowing into the inverter from the electrical system.

This example illustrates that for current flowing out of an inverter, only the clamping diodes in the top half of a phase leg will conduct, and for current flowing into an inverter, only the clamping diodes in the bottom half of the phase leg will conduct. In all likelihood the current waveforms will be odd symmetric. These facts alone enable the *average* current rating for the clamping diodes to be at most one half that of the active devices. The clamping diodes should all have a *pulse or short time* current rating equal to the amplitude of the maximum compensation current that the inverter is expected to conduct. Generally, this is equal to  $\sqrt{2}$  times the value calculated in equation (31.31) or (31.35) for the series and parallel inverters, respectively.

The average current that flows through each clamping diode is dependent on currents  $i_{SI}$  and  $i_{PI}$ , the modulation index, and the control of the voltage level outputs of the inverter. Because all of these are widely varying attributes in a power conditioner, an explicit formula for determining their ratings would be difficult at best. Nonetheless, for the assumption that each clamping diode conducts an equal amount of current and that each level of the inverter is “on” for an equal duration of time, their average current ratings for the series and parallel inverter could be found from the following equations:

$$I_{SI_{clamping diode device rating}} = \frac{I_{SI_{device rating}}}{2 \cdot (m-1)}, \text{ or} \quad (31.36)$$

$$\frac{I_{PI}}{I_{PI}_{clamping}} = \frac{\frac{I_{PI}}{device rating}}{2 \cdot (m-1)} . \quad (31.37)$$

### 31.4.6 DC link capacitor specifications

Unipolar capacitors can be used for the dc link capacitors. Just like the voltage rating of the active devices in (31.22), the sum of the voltage ratings of the dc link capacitors should be greater than or equal to the overall dc link voltage which is equal to the right side of (31.22). The design factor in this case would include the dc link voltage ripple plus any safety factor the designer feels is necessary to maintain the capacitors within their safe operating range.

The capacitance of each capacitor in the dc link is determined by the equation

$$C_n = \frac{\Delta q_n}{\Delta V_n} , \quad (31.38)$$

where  $n = 1, 2, 3, \dots, m-1$ ,  $\Delta q_n$  is the change in charge, and  $\Delta V_n$  is the change in voltage over a specified period.

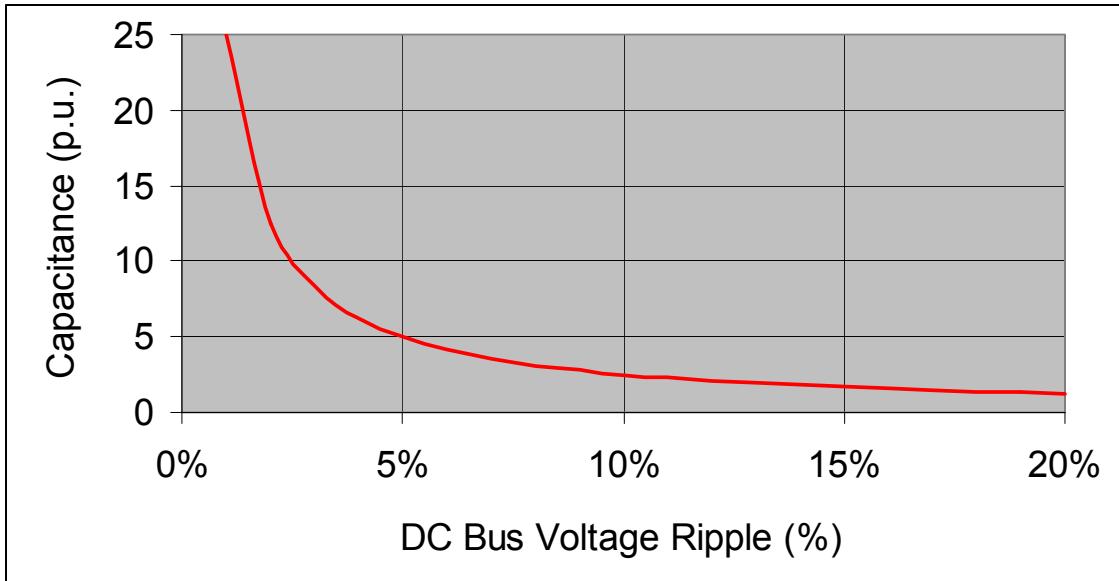
The required capacitance of the dc link and the voltage ripple are inversely related to each other. An increase in the capacitance will decrease the amount of ripple in the dc voltage. By assuming that each level has the same voltage  $V_{dc}$  across it,

$$\Delta V_n = \%V_{ripple} \cdot V_{dc} . \quad (31.39)$$

Figure 31.32 shows a graph of the required capacitance as a function of the maximum permissible voltage ripple on the dc link. The graph indicates that an unnecessarily strict tolerance on the voltage ripple of the dc bus will result in extraordinarily large capacitor values. For this reason, the maximum voltage ripple is normally chosen to be in the 5 to 10% range.

The current that flows through the capacitor determines the change in charge  $\Delta q_n$  for a capacitor  $C_n$ . This current is a function of what input and output voltage states the inverter progresses through during each cycle, and will largely be dependent on the control method implemented by the series and parallel inverter in maintaining the voltage on the dc link. In addition, the current waveforms  $i_{PI}$  and  $i_{SI}$  also will depend largely on the system conditions, in other words, the type of compensation that the converter is conducting. Although the current that flows through each capacitor  $C_n$  that makes up the dc link will be different, for the reasons mentioned previously in section 31.4.2, normally each of the capacitors will be identically sized such that (31.38) can then be rewritten as

$$C_n = C_{dc} = \frac{\max(\Delta q_n)}{\%V_{ripple} \cdot V_{dc}} . \quad (31.40)$$



**Figure 31.32.** Capacitance required as a function of the maximum voltage ripple on dc bus.

From (31.22),  $V_{device \cdot rating} \cdot (m-1) \geq \sqrt{2} \cdot 7970 \cdot 1.5 = 16900V$ . If 3300V IGBTs are chosen for the

design, then the number of levels  $m$  would be 6. The next lower rating of available IGBTs is 2500 V, and use of these devices would require 7 levels. Because of the added complexity and computational burden of 7 levels, the design with 6 levels of 3300 V IGBTs is chosen.

A 13.8 kV line-line ac waveform from an inverter requires a minimum dc link voltage of approximately 11.3 kV. The nominal dc voltage for each level would be approximately 2000 V. For a design factor of 1.5, the design voltage for each level of the inverter would be approximately 3000V.

From (31.23), the minimum total voltage blocking capability for a back-to-back converter would be,  $V_{clamp \cdot total} = 6 \cdot (6-2) \cdot (6-1) \cdot 3000V = 360kV$ . Each phase of the converter will require the blocking voltages shown in Table 31.7.

**Table 31.7.** Back-to-back MUPC clamping diode ratings.

Per Unit Voltage Rating	Blocking Voltage Required	Voltage Rating of Diode Used	# of Diodes Per Leg	Total # Per Phase
$1 \cdot V_{dc}$	3000V	3000V	1	2
$2 \cdot V_{dc}$	6000V	3000V	2	4
$3 \cdot V_{dc}$	9000V	3000V	3	6
$4 \cdot V_{dc}$	12000V	3000V	4	8

The current rating of the active devices in the series inverter is found from (31.31):

$$I_{SI_{device rating}} = \frac{20MVA \cdot \left( \frac{1}{1-0.3} - 1 \right)}{\sqrt{3} \cdot 13800V} \cdot 1.5 = 540A$$

The current rating of the active devices in the parallel inverter is found from (31.35):

$$I_{PI_{device rating}} = \frac{20MVA \cdot (1 - 0.85^2)^{1/2}}{\sqrt{3} \cdot 13800V} \cdot 1.5 = 661A$$

Use of 3300V, 800A IGBTs would be sufficient for both the series and parallel inverter. The current rating of the clamping diodes in the series inverter is found from (31.36):

$$I_{SI_{clamping diode}} = \frac{540A}{2 \cdot (6-1)} = 54A$$

Likewise, the current rating of the clamping diodes in the parallel inverter is found from (31.37):

$$I_{PI_{clamping diode}} = \frac{660A}{2 \cdot (6-1)} = 66A$$

Use of 3000V, 75A diodes would be sufficient for both the series and parallel inverter.

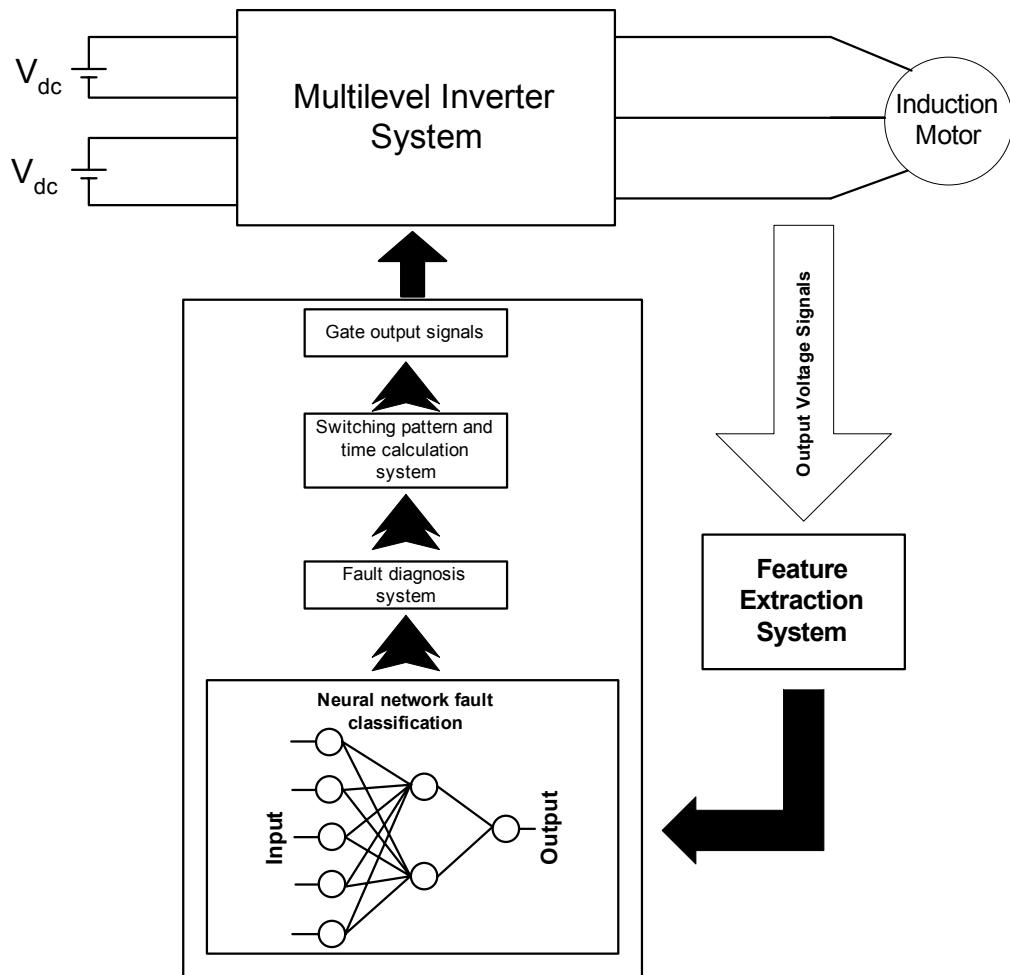
## 31.5 Fault diagnosis in multilevel converters

Since a multilevel converter is normally used in medium to high power applications, the reliability of the multilevel converter system is very important. For instance industrial drive applications in manufacturing plants are dependent upon induction motors and their inverter systems for process control. Generally, the conventional protection systems are passive devices such as fuses, overload relays, and circuit breakers to protect the inverter systems and the induction motors. The protection devices will disconnect the power sources from the multilevel inverter system whenever a fault occurs, stopping the operated process. Downtime of manufacturing equipment can add up to be thousands or hundreds of thousands of dollars per hour, therefore fault detection and diagnosis is vital to a company's bottom line. In order to maintain continuous operation for a multilevel inverter system, knowledge of fault behaviors, fault prediction, and fault diagnosis are necessary. Faults should be detected as soon as possible after they occur, because if a motor drive runs continuously under abnormal conditions, the drive or motor may quickly fail.

The possible structure for a fault diagnosis system is illustrated in Figure 31.33. The system is composed of four major states: feature extraction, neural network classification, fault

diagnosis, and switching pattern calculation with gate signal output. The feature extraction performs the voltage input signal transformation, with rated signal values as important features, and the output of the transformed signal is transferred to the neural network classification. The networks are trained with both normal and abnormal data for the MLID; thus, the output of this network is nearly 0 and 1 as binary code. The binary code is sent to the fault diagnosis to decode the fault type and its location. Then, the switching pattern is calculated to reconfigure the multilevel inverter.

Switching patterns and the modulation index of other active switches can be adjusted to maintain voltage and current in a balanced condition after reconfiguration recovers from a fault. The MLID can continuously operate in a balanced condition; of course, the MLID will not be able to operate at its rated power. Therefore, the MLID can operate in balanced condition at reduced power after the fault occurs until the operator locates and replaces the damaged switch [76].

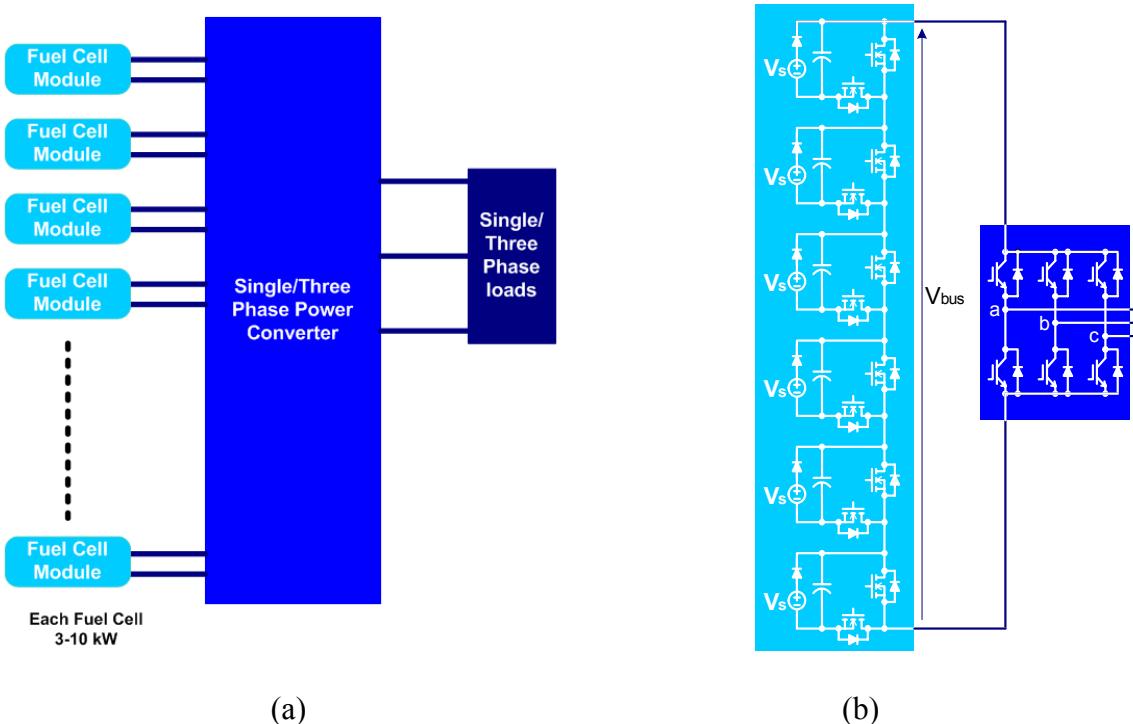


**Figure 31.33.** Structure of fault diagnosis system of a multilevel cascaded H-bridges inverter.

## 31.6 Renewable energy interface

Multilevel converters can be used to interface with renewable energy and/or distributed energy resources because several batteries, fuel cells, solar cells, wind turbines, and micro turbines can be connected through a multilevel converter to supply a load or the ac grid without voltage balancing problems. Nevertheless, the intrinsic characteristics of renewable energy sources might have some trouble with their energy source utilization; for instance, fuel cell energy sources have some problems associated with their V-I characteristics. The static V-I characteristic of fuel cells illustrates more than 30% difference in the output voltage between no-load and full load condition. This unavoidable decrease, caused by internal losses reduces fuel cell utilization factor. Therefore, a multilevel DC-DC converter might be used to overcome the problem as shown in Figure 31.34. To overcome the fuel cell voltage drop, either voltage regulators have to be connected at the fuel cell outputs or fuel cell voltages have to be monitored and the control signals have to be modified accordingly.

Five different approaches for integrating numerous fuel cell modules have been evaluated and compared with respect to cost, control complexity, ease of modularity, and fault tolerance in [77]. In addition, the optimum fuel cell utilization technique with a multilevel DC-DC converter has been proposed in [78-79].



**Figure 31.34** (a) Block diagram of the multilevel configuration, (b) 6-level dc-dc converter connected with three-phase conventional inverter.

## 31.7 Conclusion

This chapter has demonstrated the state of the art of multilevel power converter technology. Fundamental multilevel converter structures and modulation paradigms including the pros and cons of each technique have been discussed. Most of the chapter focus has addressed modern and more practical industrial applications of multilevel converters. A procedure for calculating the required ratings for the active switches, clamping diodes, and dc link capacitors with a design example has been described. The possible future enlargements of multilevel converter technology such as fault diagnosis system and renewable energy sources have been noted. It should be noted that this chapter could not cover all multilevel power converter related applications, however the basic principles of different multilevel converters have been discussed methodically. The main objective of this chapter is to provide a general notion to readers who are interested in multilevel power converters and their applications.

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