1 CMOS Ampifier

The voltage and resistance values used in this exercise are $V_{DD} = 8V$, $V_{SS} = -8V$ and $R_L = 12\text{k}\Omega$. First, we begin by determining the frequency range in which the amplifier operates normally by graphing a Bode-plot. This gives us a cutoff frequency of approximately 800kHz. With this information we can pick an appropriate frequency to examine the amplification at, in this case 1kHz.

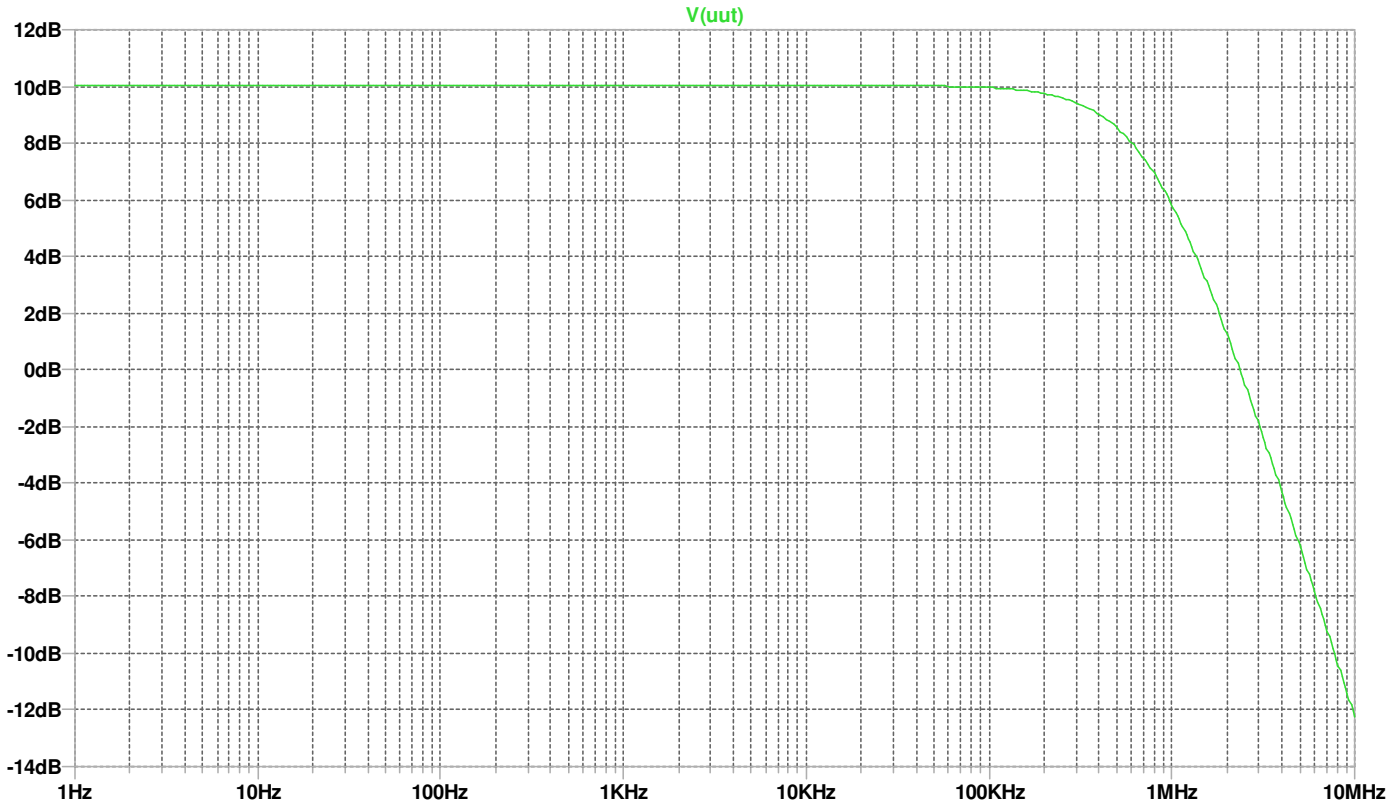

Figure 1: *Frequency response of the CMOS amplifier @ 1V input signal.*

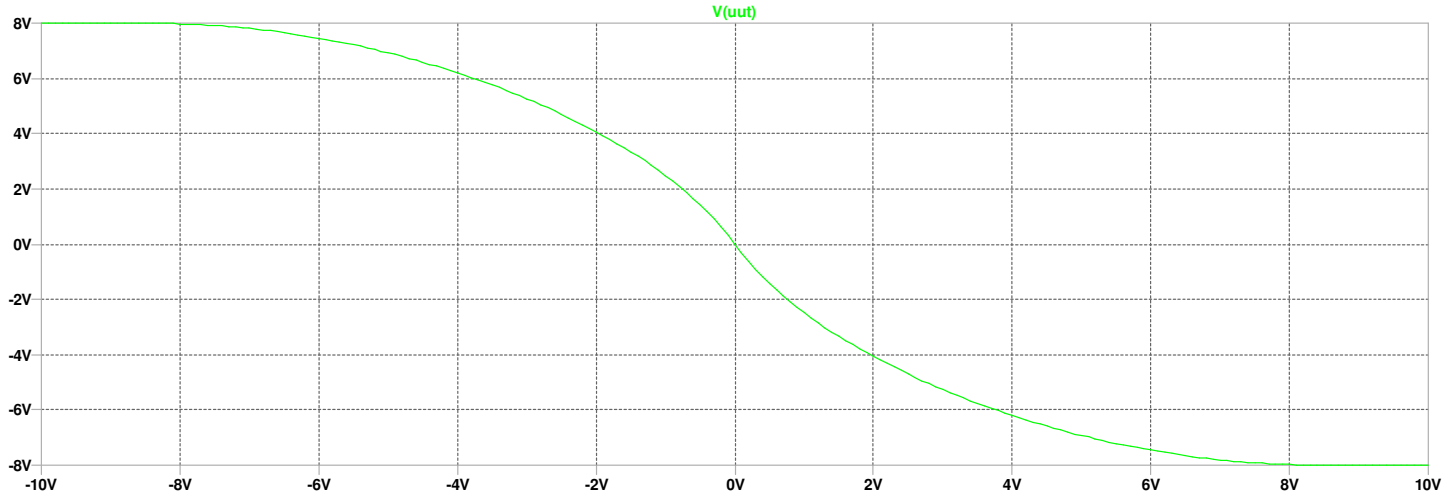

Figure 2: U_{ut} vs. U_{in}

2 CMOS Inverter

The delay on U_{ut} when transitioning from -8V to 8V is approximately 470ns. This gives a theoretical maximum frequency of

$$(2 \cdot 470ns)^{-1} \approx 1.06\text{MHz}$$

In an 'idle' state the transistors draw approx. 4mA, whereas the maximum current draw during a transition is approx. 810mA.

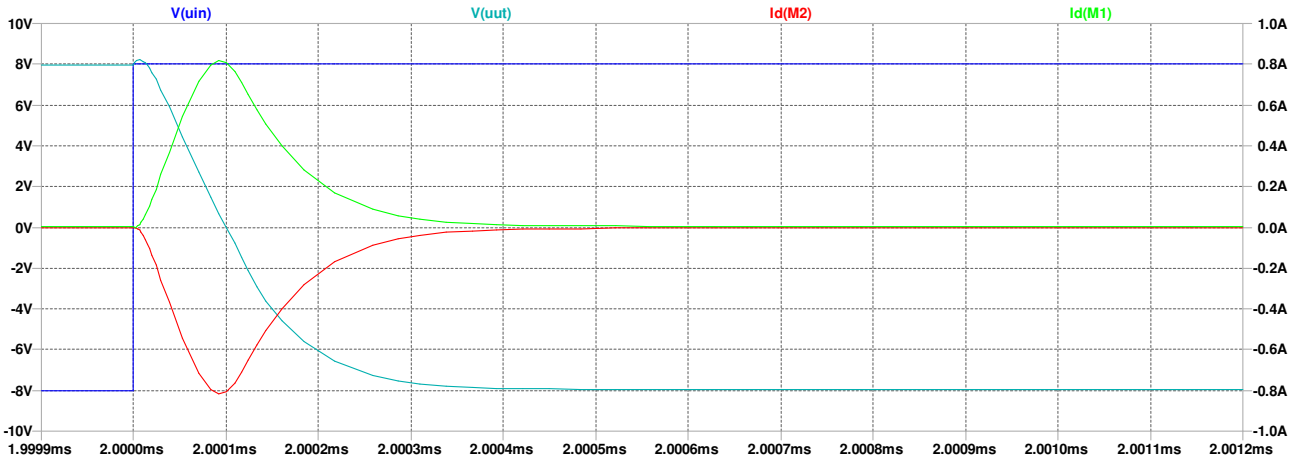

Figure 3: *The graph shows the transition delay from Uin to Uut as well as the current draw in both transistors. Note that current is only drawn during the transition.*

Since the current draw is small during the idle period and only increases during the 470ns transitions, and averages less than half of the peak current draw, we can conclude that the average power consumption will be almost insignificant (although the not insignificant peak current may have to be accounted for depending on the application) .