designed and inserted at the interface to serve as an "impedance converter". Detailed coverage of the art of matching network design is beyond the scope of this book; nevertheless, in the following sections, some of the basic concepts of matching network design is introduced by means of examples.

For sake of clarifying the terminology, it is important that we distinguish between two similar, and therefore often confused, circuit design activities: impedance transformation and impedance matching.

Impedance transformation is used to transform one impedance to a different value. At the output node of the transformation network, the new impedance is visible and it effectively masks the impedance connected to the input node of the transformation network. This interface is always unidirectional and is intended to interface only one impedance with the rest of the system.

Impedance matching is always performed between two impedances. The interface is always bidirectional and intended to maximize power transfer between the two impedances. In this book, unless otherwise specified, we design the inserted matching network with the goal of maximizing signal power transfer.

6.5 Impedance Transformation

In Sect. 4.1.7.2 and (4.59), we introduced loaded transformers. For convenience, we repeat here the important voltage–current relationship between the primary and secondary coils,

$$v_s i_s = v_p i_p, \tag{6.13}$$

which implies that in a transformer coil, increase in the coil voltage is accompanied by decrease in the coil current. Effectively, a transformer presents an impedance at its primary side that is different from the impedance of the load.

$$Z_p = \left(\frac{N_p}{N_s}\right)^2 Z_s, \tag{6.14}$$

which states that ratio of the primary and secondary impedances is equal to the square of the primary and secondary coil turns ratio. In other words, impedance Z_L at the secondary coil is "seen" at the primary coil as $(N_p/N_s)^2 R_L$. For this property alone, transformers are often used as impedance converters in RF circuits.

6.6 The Q Matching Technique

This impedance matching technique is based on the idea that a single L-shaped (X_S,X_P) branch is sufficient to provide impedance transition between two real, unequal resistances R_0 and R_L. When the two resistances are already equal, i.e., $R_0 = R_L$, there is no need for additional matching. We observe that by looking into the connecting node ① in Fig. 6.3, towards the source we see the same impedance as when looking at the load.

When the two matching resistances are not equal $R_0 \neq R_L$, we intuitively try to equalize the two sides at node ① by adding serial reactance X_S to the side with the lower initial resistance and, at the same time, by adding parallel reactance X_P to the side with the higher initial resistance. Of course, we are exploiting the fact that addition of a serial resistance increases the overall branch resistance, while addition of a parallel resistance reduces the overall branch resistance.

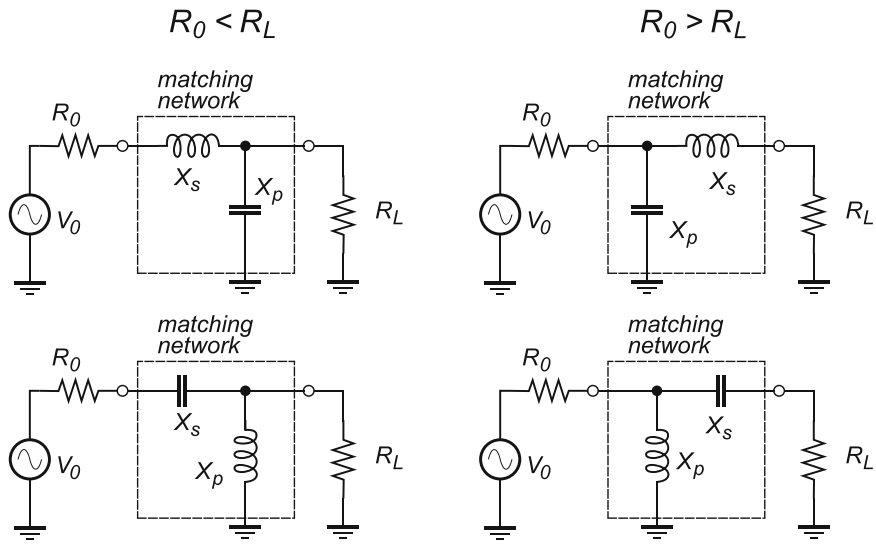

Fig. 6.4 Four ways to use a single X_0–X_P circuit branch as a matching network between the source resistance R_0 and the load resistance R_L. On the *left*, $R_0 < R_L$; on the *right*, $R_0 > R_L$

Because there are only two initial resistances to compare, R_0 and R_L, and two possible flavours of reactances that can be used $(j\omega L)$ and $(1/j\omega C)$, there are only four possible combinations that can be made. On the left of Fig. 6.4 either inductive or capacitive reactance X_S is used in series with $R_0 < R_L$. At the same time, either capacitive or inductive reactance X_P is used in parallel with load resistance $R_L > R_0$. The rule is that the two reactive components X_S and X_P must not be of the same type, i.e., one must be inductive and the other capacitive. Similarly, on the right of Fig. 6.4, either capacitive or inductive reactance is used in parallel with the source resistance $R_0 > R_L$ and either inductive or capacitive reactance is used in series with $R_L < R_0$.

At this point it is valid to ask why we use reactances when the same goal is achievable with a resistive network. It is possible to design a matching network using only resistors, however the power loss increases drastically and wideband networks are always much noisier, which reduces SNR. For each of the two relations between $R_0 \lessgtr R_L$, there two possible matching networks; we may ask if there is any difference between the two. If there are no additional constraints, either solution is valid. For example, either of the two matching networks on the left of Fig. 6.4 is valid when $R_0 < R_L$. In practice, we usually have additional constraints, for example, if a DC connection needs to be maintained between the source and load resistance then the serial reactance must be inductive, $X_S = j\omega L$ (the upper two cases in Fig. 6.4); if an AC connection is desired, the serial reactance must be capacitive, $X_S = 1/j\omega C$ (the lower two cases in Fig. 6.4).

6.6.1 Matching Real Impedances

A typical matching problem involves only real source and load resistances that are not equal, $R_0 \neq R_L$. For example, in Fig. 6.5, source resistance $R_0 = 5\,\Omega$ must drive a load of $R_L = 50\,\Omega$. After the matching network is designed and inserted, the source should "see" a load value of, in this case, $5\,\Omega$ and, at the same time, the load resistor should "feel" as if it was driven by a source resistance equal to its own, in this example $50\,\Omega$. Let us find out how a general problem such as this one is solved using the Q matching technique. As a side note, one of the drawbacks of this technique is its use of reactive components, meaning that the matching is possible at only one frequency.

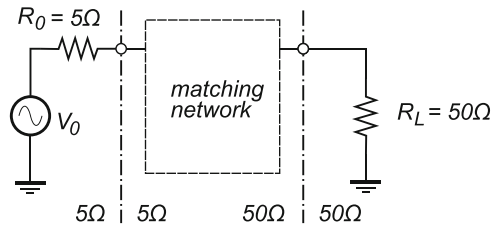

Fig. 6.5 A typical case of mismatched source and load resistances, $R_0 < R_L$

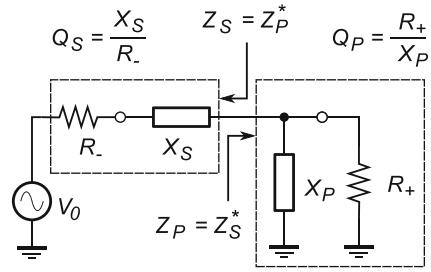

Fig. 6.6 An LC section placed between two resistive terminations creates a serial subnetwork and a parallel subnetwork. When the two subnetworks are conjugate matched to each other, their Q factors are equal

If we apply knowledge about serial–parallel transformations of resonant LC networks (see Sect. 5.5), the matching network design procedure is summarized by four simple steps[1]:

1. Add a series reactive element X_S next to R_- and increase the impedance of the serial subnetwork branch. Add a parallel reactive element X_P next to R_+ and reduce the impedance of the parallel subnetwork branch. We note that, if the serial element is an inductor, adding a parallel capacitor creates a LP topology (see Fig. 6.6); a serial capacitor in combination with a parallel inductor forms a high-pass section.
2. At the design frequency, the two newly created subnetworks, one in series and one in parallel (Fig. 6.6), must represent complex conjugate impedances to each other. Thus, the Q factors of these two subnetworks must be equal at the frequency where the match is computed. The serial Q factor Q_S and the parallel Q factor Q_P of the two subnetworks are

$$Q_S = \frac{X_S}{R_-} \quad \text{and} \quad Q_P = \frac{R_+}{X_P}. \tag{6.15}$$

3. Using (5.79) and (5.80) we calculate the serial and parallel Q factors of the two subnetworks as

$$Q_S = Q_P = \sqrt{\frac{R_+}{R_-} - 1}. \tag{6.16}$$

4. Once the Q factors are calculated, the next step is to calculate the series and parallel reactances from (6.15) and to compute the inductor and capacitor values by using their respective impedance definitions for the given design frequency.

In summary, the Q matching methodology for the case of signal source V_0 with real source resistance R_0 (either R_- or R_+) that drives a load with real resistance R_L (either R_+ or R_-) is a straightforward procedure because there are only four possible matching networks to consider. In order

[1] In order to better visualize the design steps, the lower of the two resistances is labelled R_- while the higher of the two is labelled R_+.

to make the solution unique, an additional constraint must be introduced to further determine the nature of serial and parallel impedances in the matching network. For example, if the matching network is to preserve a DC connection between the source and the load, then an inductor must be chosen as the serial element. Similarly, if an AC connection between the source and the load is to be preserved, a capacitor must be chosen as the serial element.

Example 6.1. Using the Q matching technique, design a single-section LC network to match a source resistance $R_0 = 5\,\Omega$ to a resistive load $R_L = 50\,\Omega$ at $f = 100\,\text{MHz}$ (see Fig. 6.5). Maintain a DC connection between the source and the load.

Solution 6.1. The source resistance is smaller than the load resistance, $R_S < R_L$, hence, $R_S = R_-$ and $R_L = R_+$ (Figs. 6.5 and 6.6). Therefore, serial reactance needs to be added to the source resistance R_- and parallel reactance to the load resistance R_+. Adding a serial inductor to the $5\,\Omega$ source side and a parallel capacitor to the $50\,\Omega$ load side keeps the DC connection and creates the LP matching configuration.

From (6.16), the required Q factors are calculated as

$$Q_S = Q_P = \sqrt{\frac{R_+}{R_-} - 1} = \sqrt{\frac{50}{5} - 1} = 3.$$

From (6.15) it follows, first for the serial component,

$$X_S = Q_S R_- = 3 \cdot 5\,\Omega = 15\,\Omega,$$

$$\therefore$$

$$L = \frac{15\,\Omega}{2\pi\,100\,\text{MHz}} = 23.873\text{nH}$$

and then for the parallel component,

$$X_P = \frac{R_+}{Q_P} = \frac{50\,\Omega}{3} = 16.667\,\Omega,$$

$$\therefore$$

$$C = \frac{1}{2\pi\,100\,\text{MHz}\,16.667\,\Omega} = 95.491\,\text{nF}.$$

Let us verify the above result. After inserting the matching network and looking into the source side (Fig. 6.6), there is a serial connection of the source resistance R_0 and the matching network's inductor X_S. Therefore, the total serial source side impedance is $|Z_0| = \sqrt{R_0^2 + X_S^2} = \sqrt{5^2 + 15^2}\,\Omega = 15.811\,\Omega$. At the same time, looking into the load side, there is a parallel connection of R_L and X_P. Therefore, the parallel impedance at the load side is $|Z_L| = 1/\sqrt{1/R_L^2 + 1/X_P^2} = 1/\sqrt{1/50^2 + 1/16.667^2}\,\Omega = 15.811\,\Omega$. Thus, the source side impedance has increased and the load side impedance has decreased, with the apparent matching of the two sides at $15.811\,\Omega$.

Example 6.2. Match a $50\,\Omega$ resistive source at 100 MHz to a load that is a serial connection of a $50\,\Omega$ resistor and a 95.491 nF capacitance.

Solution 6.2. This is a trivial case because the real parts of the source and load impedances are equal. Because the load side has an additional $X_S = -15\,\Omega$, the required matching circuit is simply

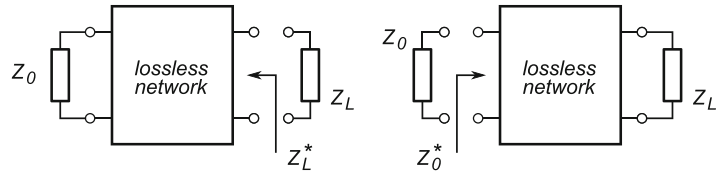

Fig. 6.7 Matching complex impedances by design of the lossless matching network simultaneously provides bidirectional complex conjugate matching

an inductor in series with the source resistance R_s, i.e., $X_L = +15\,\Omega$, therefore $L = 23.873\,\text{nH}$. At $f = 100\,\text{MHz}$, the serial connection of the inductor and the capacitor results in zero impedance, which leaves the two real resistances matched.

6.6.2 Matching Complex Impedances

A general case of matching complex impedances follows the same design methodology presented in the previous sections, i.e., properly designed matching network must provide correct complex conjugate matching both at the input terminal plane and at the output terminal plane. When looking into the output terminals of the matching networks we need to see the complex conjugate value of the output impedance and when looking into the input terminals of the matching network we need to see the complex conjugate value of the input impedance (Fig. 6.7). Under those conditions, all of the signal power is delivered to the load without any reflection at the output port.

The reactances associated with source and load impedances are referred to as "parasitics". If any of the two matching impedances Z_0 and Z_L already contains parasitics, the matching network design problem can be approached in two possible ways that may lead to the desired solution: we could try to "absorb the parasitics" into the matching network or to eliminate the parasitics by resonance, i.e to "resonate them out". In both of these methods, the parasitic reactances may be eliminated either completely or partially. A design procedure for matching complex impedances starts by solving the matching network for the real parts and then proceeds by absorbing the parasitics or resonating them out, either completely and partially.

6.6.2.1 Absorbing the Parasitics

Let us consider a case where source or load impedances include parasitic reactances. In addition, let us assume that values of the parasitic reactances are lower than the component values of the matching network that is required to match only the real parts of the two impedances. If that is the case, there is an opportunity to "absorb" i.e., to combine, these source or load parasitics with the matching network components. Let us take a look at the following example.

Example 6.3. Design a single-stage LC matching network at $f = 100\,\text{MHz}$ for the case of a source V_0 whose impedance consists of a resistor $R_0 = 5\,\Omega$ connected in series with an $L_S = 13.873\,\text{nH}$ inductor, which has to drive an $R_L = 50\,\Omega$ load resistance in parallel with $C_L = 45.491\,\text{nF}$, Fig. 6.8 (left). The matching network is expected to maintain a DC path between the source and the load.

Solution 6.3. In the case of a source or load with complex impedances, a good starting point is to first resolve the matching network only for the real parts of the two impedances. In Example 6.1,

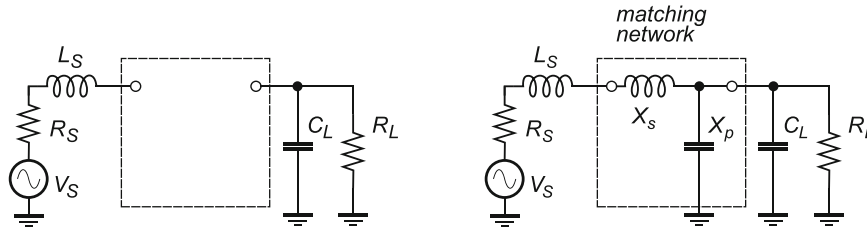

Fig. 6.8 Complex source with impedance $Z_0 = R_0 + j\omega L_S$ is required to drive a load with impedance $Z_L = R_L||1/j\omega C_L$ (*left*). Both the source and the load reactive parasitics are absorbed by the matching network (*right*)

we designed a matching network for the case of real $R_0 = 5\,\Omega$ source and $R_L = 50\,\Omega$ load at 100 MHz, which happen to be numerically equal to the real parts of the impedances in this example. Hence, we reuse the results and treat those calculations as the first phase of this example.

As we already found in Example 6.1, to match $R_0 = 5\,\Omega$ to $R_L = 50\,\Omega$ we need an $X'_S = 23.873\,\text{nH}$ inductor and an $X'_P = 95.491\,\text{nF}$ capacitor. However, the source impedance in this example already contains $L_S = 13.873\,\text{nH}$ inductance, which means that only the additional $X_S = 23.873\,\text{nH} - 13.873\,\text{nH} = 10\,\text{nH}$ inductor in series is needed, as shown in Fig. 6.8 (right). By doing this, we "absorb" the existing parasitic inductance into the value of the inductance required by the matching network. At the same time, the loading impedance needs a total of $X'_P = 95.491\,\text{nF}$ capacitance, which means that only the additional $X_P = 95.491\,\text{nF} - 45.491 = 50\,\text{nF}$ capacitor is needed in parallel with the existing $C_L = 45.491\,\text{nF}$ parasitic capacitance. By doing this, we "absorb" the existing parasitic capacitance into the value of the capacitance required by the matching network. Therefore, the required matching network consists of an $X_S = 10\,\text{nH}$ inductor and an $X_P = 50\,\text{nF}$ capacitor, as shown in Fig. 6.8 (right), i.e., $L_S + X_S = 23.873\,\text{nH}$ and $C_L + X_P = 95.491\,\text{nF}$.

6.6.2.2 Resonating out Excessive Parasitics

Let us consider a case where, for example, the load impedance includes parasitic reactance. In addition, let us assume that value of the parasitic reactance is greater than the value of the component of the matching network designed to match only the real parts of the two impedances. If that is the case, there is an opportunity to "resonate out", either fully or partially, the load's parasitic reactance with the matching network's components. To illustrate the point, let us reuse the results of the previous examples.

Example 6.4. Design a single-stage LC matching network at $f = 100\,\text{MHz}$ for the case of a source V_0 with a $R_0 = 5\,\Omega$ output resistance, which has to drive a $R_L = 50\,\Omega$ load resistance in parallel with $C_L = 105.491\,\text{nF}$. The matching network is expected to maintain a DC path between the source and the load.

Solution 6.4. As we already found in Example 6.1, to match $R_0 = 5\,\Omega$ to $R_L = 50\,\Omega$ we need $X'_S = 23.873\,\text{nH}$ inductor and $X'_P = 95.491\,\text{nF}$ capacitor. However, the source impedance already includes the parasitic capacitance of $C_L = 105.491\,\text{nF}$, which means that somehow we need to reach the required $X'_P = 95.491\,\text{nF}$. In general, there are two possible ways to approach this kind of problem.

- *Total resonating out*: Let us first create an LC resonator that consists of the existing parasitic capacitance C_L in parallel with an inductor L_L (a new component). If we set the resonant frequency of this LC resonator to $f_0 = 100\,\text{MHz}$, we create (in the ideal case) dynamic impedance $R_D = \infty$ in parallel to the load resistance R_L. Consequently, the total loading impedance becomes

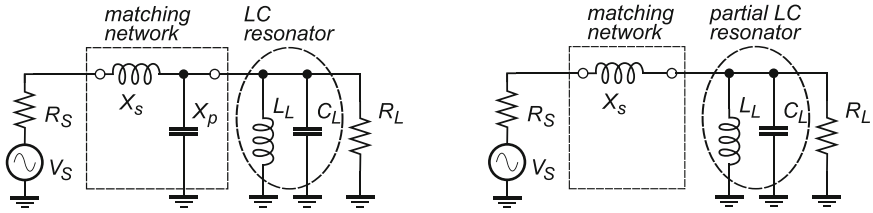

Fig. 6.9 Parasitic load capacitance C_L is completely "resonated out" by adding parallel inductor L_L (*left*). Only the excess amount of parasitic capacitance C_L is "partially resonated out" (i.e. its effective size is reduced) by adding parallel inductance L_L (*right*)

$Z_L = R_L || R_D = R_L$, i.e., the parasitic capacitance is "resonated out" and, effectively, disappears. In this case, we would need to use an $L_L = 24.024\,\text{pH}$ inductor. Although it is very difficult to create such a small inductor, for sake of argument let us keep the numbers. Once the parasitic capacitance is fully resonated out, we are back to the problem of Example 6.1, which means that, in order to finalize the matching network, we need to add an $X_S = 23.873\,\text{nH}$ inductor and an $X_P = 95.491\,\text{nF}$ capacitor, as shown in Fig. 6.9 (left). This solution requires three new components: X_S, X_P, and L_L.

- *Partial resonating out*: Let us try to resonate out only the excess part of the parasitic capacitance, i.e., $C'_L = C_L - X'_P = 105.491\,\text{nF} - 95.491\,\text{nF} = 10\,\text{nF}$. That is, let us create an LC resonator that consists of the existing part of the parasitic capacitance C'_L in parallel with an inductor L_L (a new component), so that they resonate at $f_0 = 100\,\text{MHz}$. To do so, we need $L_L = 1/(2\pi f_0)^2 C'_L = 252.3\,\text{pH}$. By adding the new component, the L_L inductor, in parallel with the parasitic capacitance, we effectively reduce the size of the capacitor. One way to visualize this situation is to imagine that the load capacitance C_L consists of two capacitors in parallel, i.e., $C_L = 95.491\,\text{nF} + 10\,\text{nF}$. The newly created LC resonator resonates out the 10 nF part and becomes effectively infinite dynamic impedance $R_D = \infty$. Hence, the 95.491 nF capacitance required by the matching network is still available – all we need to do is to add the series inductance $X'_S = 23.873\,\text{nH}$, as shown in Fig. 6.9 (right). Therefore this solution requires only the two new components, L_L and X_0. And, as a side note, in this solution the resonating inductor is a bit larger.

6.7 Bandwidth of a Single-Stage LC Matching Network

So far in our discussion of single-stage LC matching networks, we have only focused on the main goal of matching the source side impedance to the load side impedance. We had no freedom to control the bandwidth of the overall network. We have learned by now that a general RLC network always behaves as a bandpass filter centred around the resonant frequency ω_0, which is determined by the LC components. We also have learned that, as a good approximation (assuming Q factor larger than ten or so), the serial and parallel RLC networks resonate in the same way. Therefore, it is very important to estimate the bandwidth of matched networks, because we may reach a solution that offers too wide a bandwidth (and allows too much noise into the system) or too narrow a bandwidth (and alters the frequency content of the passing signals, i.e., the matching network distorts the signal).

A more detailed network analysis, which is beyond the scope of this book, would have revealed that determining the network bandwidth using the standard definition based on the 3 dB points turns out to be problematic, to say the least. There are at least two good reasons for this statement. One has to do with the fact that some resonant networks may never reach the 3 dB attenuation points. For example, a low Q resonant curve is almost flat—it may not even have 3 dB difference between its maximum amplitude at the point of the resonant frequency and the side points. A second, and less obvious, reason for our difficulties in determining the 3 dB bandwidth of LC matching networks