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S12CRGV3/D

CRG
Block User Guide
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Section 1 Introduction

1.1 Overview

This specification describes the function of the Clocks and Reset Generator (CRG).

1.2 Features

The main features of this block are:

- Crystal (or ceramic resonator) oscillator (OSC)
  - User selectable Oscillator type: Colpitts (low power) or Pierce
  - Clock monitor (CM)
  - Startup counter
- Phase Locked Loop (PLL) frequency multiplier
  - Reference divider
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - CPU interrupt on entry or exit from locked condition
  - Self Clock Mode in absence of reference clock
- System Clock Generator
  - External clock mode
  - System clock switch
  - System clocks off during Wait Mode
- System Reset Generator
  - Computer Operating Properly (COP) watchdog timer with time-out clear window.
  - Loss of clock reset
  - External pin reset
- Real-Time Interrupt (RTI)

1.3 Modes of Operation

This subsection lists and briefly describes all CRG operating modes supported by the CRG. This is a high level description only, detailed descriptions of operating modes are contained in later sections.

- Run Mode

All functional parts of the CRG are running during normal Run Mode. If RTI or COP functionality is required the individual bits of the associated rate select registers (COPCTL, RTICTL) have to be set to a non zero value[1].

- Wait Mode

  Depending on the configuration of the individual bits in the CLKSEL register this mode allows to disable the system and core clocks.

- Stop Mode

  Depending on the setting of the PSTP bit Stop Mode can be differentiated between Full Stop Mode (PSTP=0) and Pseudo Stop Mode (PSTP=1).

  – Full Stop Mode

    The oscillator is disabled and thus all system and core clocks are stopped. The COP and the RTI remain frozen.

  – Pseudo Stop Mode

    The oscillator continues to run and most of the system and core clocks are stopped. If the respective enable bits are set the COP and RTI will continue to run, else they remain frozen.

- Self Clock Mode

  Self Clock Mode will be entered if the Clock Monitor Enable Bit (CME) and the Self Clock Mode Enable Bit (SCME) are both asserted and the clock monitor detects a loss of clock (external oscillator or crystal). As soon as Self Clock Mode is entered the CRG starts to perform a clock check. Self Clock Mode remains active until the clock check indicates the required quality of the incoming clock signal is met (frequency and amplitude). Self Clock Mode should be used for safety purposes only. It provides reduced functionality to the MCU in case a loss of clock is causing severe system conditions.

1.4 Block Diagram

Figure 1-1 shows a block diagram of the CRG.

NOTES:
1. COPCTL register is write once only

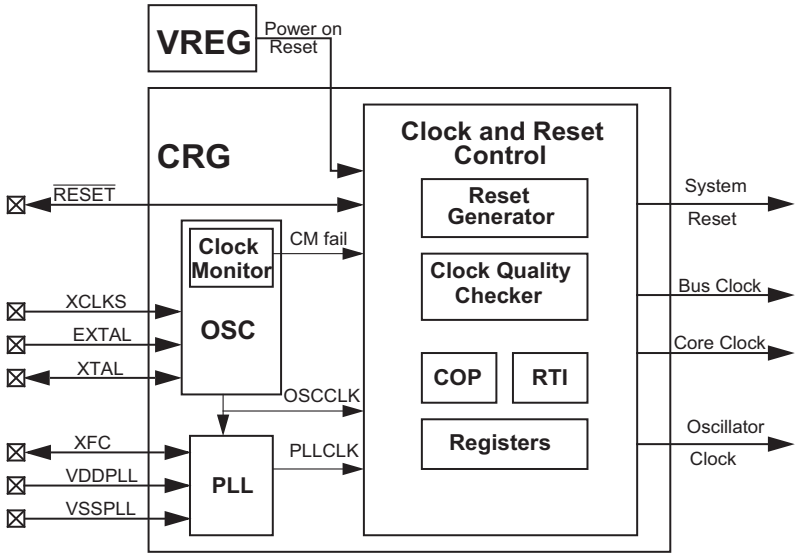

Figure 1-1 Block diagram of CRG

Section 3 Memory Map and Registers

3.1 Overview

This section provides a detailed description of all registers accessible in the CRG.

3.2 Module Memory Map

Table 3-1 gives an overview on all CRG registers.

Table 3-1 CRG Memory Map

Address Offset	Use	Access
$_00	CRG Synthesizer Register (SYNR)	R/W
$_01	CRG Reference Divider Register (REFDV)	R/W
$_02	CRG Test Flags Register (CTFLG)[1]	R/W
$_03	CRG Flags Register (CRGFLG)	R/W
$_04	CRG Interrupt Enable Register (CRGINT)	R/W
$_05	CRG Clock Select Register (CLKSEL)	R/W
$_06	CRG PLL Control Register (PLLCTL)	R/W
$_07	CRG RTI Control Register (RTICTL)	R/W
$_08	CRG COP Control Register (COPCTL)	R/W
$_09	CRG Force and Bypass Test Register (FORBYP)[2]	R/W
$_0A	CRG Test Control Register (CTCTL)[3]	R/W
$_0B	CRG COP Arm/Timer Reset (ARMCOP)	R/W

NOTES:
1. CTFLG is intended for factory test purposes only.
2. FORBYP is intended for factory test purposes only.
3. CTCTL is intended for factory test purposes only.

NOTE: *Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.*

3.3 Register Descriptions

This section describes in address order all the CRG registers and their individual bits.

3.3.1 CRG Synthesizer Register (SYNR)

The SYNR register controls the multiplication factor of the PLL. If the PLL is on, the count in the loop divider (SYNR) register effectively multiplies up the PLL clock (PLLCLK) from the reference frequency by 2 x (SYNR+1). PLLCLK will not be below the minimum VCO frequency (f_{SCM}).

$$PLLCLK = 2xOSCCLKx\frac{(SYNR+1)}{(REFDV+1)}$$

NOTE: *PLLCLK must not exceed the maximum operating system frequency.*

Address Offset: $_00

	7	6	5	4	3	2	1	0
R	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-1 CRG Synthesizer Register (SYNR)

Read: anytime

Write: anytime except if PLLSEL = 1

NOTE: *Write to this register initializes the lock detector bit and the track detector bit.*

3.3.2 CRG Reference Divider Register (REFDV)

The REFDV register provides a finer granularity for the PLL multiplier steps. The count in the reference divider divides OSCCLK frequency by REFDV+1.

Address Offset: $_01

	7	6	5	4	3	2	1	0
R	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 CRG Reference Divider Register (REFDV)

Read: anytime

Write: anytime except when PLLSEL = 1

NOTE: *Write to this register initializes the lock detector bit and the track detector bit.*

3.3.3 Reserved Register (CTFLG)

This register is reserved for factory testing of the CRG module and is not available in normal modes.

Address Offset: $_02

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-3 Reserved Register (CTFLG)

Read: always reads $00 in normal modes

Write: unimplemented in normal modes

NOTE: *Writing to this register when in special mode can alter the CRG fucntionality.*

3.3.4 CRG Flags Register (CRGFLG)

This register provides CRG status bits and flags.

Address Offset: $_03

	7	6	5	4	3	2	1	0
R	RTIF	PORF	0	LOCKIF	LOCK	TRACK	SCMIF	SCM
W								
RESET:	0	1	0	0	0	0	0	0

= Unimplemented or Reserved

NOTES:
1. PORF is set to 1 when a power on reset occurs. Unaffected by non-POR resets.

Figure 3-4 CRG Flags Register (CRGFLG)

Read: anytime

Write: refer to each bit for individual write conditions

RTIF — Real Time Interrupt Flag

RTIF is set to 1 at the end of the RTI period. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (RTIE=1), RTIF causes an interrupt request.
1 = RTI time-out has occurred.
0 = RTI time-out has not yet occurred.

PORF — Power on Reset Flag

PORF is set to 1 when a power on reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect.

1 = Power on reset has occurred.
0 = Power on reset has not occurred.

LOCKIF — PLL Lock Interrupt Flag

LOCKIF is set to 1 when LOCK status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect.If enabled (LOCKIE=1), LOCKIF causes an interrupt request.
1 = LOCK bit has changed.
0 = No change in LOCK bit.

LOCK — Lock Status Bit

LOCK reflects the current state of PLL lock condition. This bit is cleared in Self Clock Mode. Writes have no effect.
1 = PLL VCO is within the desired tolerance of the target frequency.
0 = PLL VCO is not within the desired tolerance of the target frequency.

TRACK — Track Status Bit

TRACK reflects the current state of PLL track condition. This bit is cleared in Self Clock Mode. Writes have no effect.
1 = Tracking mode status.
0 = Acquisition mode status.

SCMIF — Self Clock Mode Interrupt Flag

SCMIF is set to 1 when SCM status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (SCMIE=1), SCMIF causes an interrupt request.
1 = SCM bit has changed.
0 = No change in SCM bit.

SCM — Self Clock Mode Status Bit

SCM reflects the current clocking mode. Writes have no effect.
1 = MCU is operating in Self Clock Mode with OSCCLK in an unknown state. All clocks are derived from PLLCLK running at its minimum frequency f_{SCM}.
0 = MCU is operating normally with OSCCLK available.

3.3.5 CRG Interrupt Enable Register (CRGINT)

This register enables CRG interrupt requests.

Address Offset: $_04

	7	6	5	4	3	2	1	0
R	RTIE	0	0	LOCKIE	0	0	SCMIE	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5 CRG Interrupt Enable Register (CRGINT)

Read: anytime

Write: anytime

RTIE — Real Time Interrupt Enable Bit.
1 = Interrupt will be requested whenever RTIF is set.
0 = Interrupt requests from RTI are disabled.

LOCKIE — Lock Interrupt Enable Bit
1 = Interrupt will be requested whenever LOCKIF is set.
0 = LOCK interrupt requests are disabled.

SCMIE — Self Clock Mode Interrupt Enable Bit
1 = Interrupt will be requested whenever SCMIF is set.
0 = SCM interrupt requests are disabled.

3.3.6 CRG Clock Select Register (CLKSEL)

This register controls CRG clock selection.

Address Offset: $_05

	7	6	5	4	3	2	1	0
R	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 CRG Clock Select Register (CLKSEL)

Read: anytime

Write: refer to each bit for individual write conditions

PLLSEL — PLL Select Bit

Write anytime. Writing a one when LOCK=0 and AUTO=1, or TRACK=0 and AUTO=0 has no effect This prevents the selection of an unstable PLLCLK as SYSCLK. PLLSEL bit is cleared when the MCU enters Self Clock Mode, Stop Mode or Wait Mode with PLLWAI bit set.
1 = System clocks are derived from PLLCLK.
0 = System clocks are derived from OSCCLK.

PSTP — Pseudo Stop Bit

Write: anytime

This bit controls the functionality of the oscillator during Stop Mode.
1 = Oscillator continues to run in Stop Mode (Pseudo Stop). The oscillator amplitude is reduced.
0 = Oscillator is disabled in Stop Mode.

NOTE: *Pseudo-STOP allows for faster STOP recovery and reduces the mechanical stress and aging of the resonator in case of frequent STOP conditions at the expense of a slightly increased power consumption.*

Lower oscillator amplitude exhibits lower power consumption but could have adverse effects during any Electro-Magnetic Susceptibility (EMS) tests.

SYSWAI — System clocks stop in Wait Mode Bit

Write: anytime
1 = In Wait Mode the system clocks stop.
0 = In Wait Mode the system clocks continue to run.

NOTE: *RTI and COP are not affected by SYSWAI bit.*

ROAWAI — Reduced Oscillator Amplitude in Wait Mode Bit.

Write: anytime
1 = Reduced oscillator amplitude in Wait Mode.
0 = Normal oscillator amplitude in Wait Mode.

NOTE: *Lower oscillator amplitude exhibits lower power consumption but could have adverse effects during any Electro-Magnetic Susceptibility (EMS) tests.*

PLLWAI — PLL stops in Wait Mode Bit

Write: anytime

If PLLWAI is set, the CRG will clear the PLLSEL bit before entering Wait Mode. The PLLON bit remains set during Wait Mode but the PLL is powered down. Upon exiting Wait Mode, the PLLSEL bit has to be set manually in case PLL clock is required.

While the PLLWAI bit is set the AUTO bit is set to 1 in order to allow the PLL to automatically lock on the selected target frequency after exiting Wait Mode.
1 = PLL stops in Wait Mode.
0 = PLL keeps running in Wait Mode.

CWAI — Core stops in Wait Mode Bit

Write: anytime

1 = Core clock stops in Wait Mode.
0 = Core clock keeps running in Wait Mode.

RTIWAI — RTI stops in Wait Mode Bit

Write: anytime
1 = RTI stops and initializes the RTI dividers whenever the part goes into Wait Mode.
0 = RTI keeps running in Wait Mode.

COPWAI — COP stops in Wait Mode Bit

Normal modes: Write once

Special modes: Write anytime
1 = COP stops and initializes the COP dividers whenever the part goes into Wait Mode.
0 = COP keeps running in Wait Mode.

3.3.7 CRG PLL Control Register (PLLCTL)

This register controls the PLL functionality.

Address Offset: $_06

	7	6	5	4	3	2	1	0
R W	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
RESET:	1	1	1	1	0	0	0	1

= Unimplemented or Reserved

Figure 3-7 CRG PLL Control Register (PLLCTL)

Read: anytime

Write: refer to each bit for individual write conditions

CME — Clock Monitor Enable Bit

CME enables the clock monitor. Write anytime except when SCM = 1.
1 = Clock monitor is enabled. Slow or stopped clocks will cause a clock monitor reset sequence or Self Clock Mode.
0 = Clock monitor is disabled.

NOTE: *Operating with CME=0 will not detect any loss of clock. In case of poor clock quality this could cause unpredictable operation of the MCU!*

In Stop Mode (PSTP=0) the clock monitor is disabled independently of the CME bit setting and any loss of clock will not be detected.

PLLON — Phase Lock Loop On Bit

PLLON turns on the PLL circuitry. In Self Clock Mode, the PLL is turned on, but the PLLON bit reads the last latched value. Write anytime except when PLLSEL = 1.
1 = PLL is turned on. If AUTO bit is set, the PLL will lock automatically.
0 = PLL is turned off.

AUTO — Automatic Bandwidth Control Bit

AUTO selects either the high bandwidth (acquisition) mode or the low bandwidth (tracking) mode depending on how close to the desired frequency the VCO is running. Write anytime except when PLLWAI=1, because PLLWAI sets the AUTO bit to 1.
1 = Automatic Mode Control is enabled and ACQ bit has no effect.
0 = Automatic Mode Control is disabled and the PLL is under software control, using ACQ bit.

ACQ — Acquisition Bit

Write anytime. If AUTO=1 this bit has no effect.
1 = High bandwidth filter is selected.
0 = Low bandwidth filter is selected.

PRE — RTI Enable during Pseudo Stop Bit

PRE enables the RTI during Pseudo Stop Mode. Write anytime.
1 = RTI continues running during Pseudo Stop Mode.
0 = RTI stops running during Pseudo Stop Mode.

NOTE: *If the PRE bit is cleared the RTI dividers will go static while Pseudo-Stop Mode is active. The RTI dividers will not initialize like in Wait Mode with RTIWAI bit set.*

PCE — COP Enable during Pseudo Stop Bit

PCE enables the COP during Pseudo Stop Mode. Write anytime.
1 = COP continues running during Pseudo Stop Mode
0 = COP stops running during Pseudo Stop Mode

NOTE: *If the PCE bit is cleared the COP dividers will go static while Pseudo-Stop Mode is active. The COP dividers will not initialize like in Wait Mode with COPWAI bit set.*

SCME — Self Clock Mode Enable Bit

Normal modes: Write once

Special modes: Write anytime
SCME can not be cleared while operating in Self Clock Mode (SCM=1).
0 = Detection of crystal clock failure causes clock monitor reset (see **5.2.1 Clock Monitor Reset**).
1 = Detection of crystal clock failure forces the MCU in Self Clock Mode (see **4.3.2 Self Clock Mode**).

3.3.8 CRG RTI Control Register (RTICTL)

This register selects the timeout period for the Real Time Interrupt.

Address Offset: $_07

	7	6	5	4	3	2	1	0
R	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-8 CRG RTI Control Register (RTICTL)

Read: anytime

Write: anytime

NOTE: *A write to this register initializes the RTI counter.*

RTR[6:4] — Real Time Interrupt Prescale Rate Select Bits

These bits select the prescale rate for the RTI. See **Table 3-2**.

RTR[3:0] — Real Time Interrupt Modulus Counter Select Bits

These bits select the modulus counter target value to provide additional granularity.**Table 3-2** shows all possible divide values selectable by the RTICTL register. The source clock for the RTI is OSCCLK.

Table 3-2 RTI Frequency Divide Rates

RTR[3:0]	RTR[6:4] =							
	000 (OFF)	001 (2^{10})	010 (2^{11})	011 (2^{12})	100 (2^{13})	101 (2^{14})	110 (2^{15})	111 (2^{16})
0000 (÷1)	OFF*	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
0001 (÷2)	OFF*	$2x2^{10}$	$2x2^{11}$	$2x2^{12}$	$2x2^{13}$	$2x2^{14}$	$2x2^{15}$	$2x2^{16}$
0010 (÷3)	OFF*	$3x2^{10}$	$3x2^{11}$	$3x2^{12}$	$3x2^{13}$	$3x2^{14}$	$3x2^{15}$	$3x2^{16}$
0011 (÷4)	OFF*	$4x2^{10}$	$4x2^{11}$	$4x2^{12}$	$4x2^{13}$	$4x2^{14}$	$4x2^{15}$	$4x2^{16}$
0100 (÷5)	OFF*	$5x2^{10}$	$5x2^{11}$	$5x2^{12}$	$5x2^{13}$	$5x2^{14}$	$5x2^{15}$	$5x2^{16}$
0101 (÷6)	OFF*	$6x2^{10}$	$6x2^{11}$	$6x2^{12}$	$6x2^{13}$	$6x2^{14}$	$6x2^{15}$	$6x2^{16}$
0110 (÷7)	OFF*	$7x2^{10}$	$7x2^{11}$	$7x2^{12}$	$7x2^{13}$	$7x2^{14}$	$7x2^{15}$	$7x2^{16}$
0111 (÷8)	OFF*	$8x2^{10}$	$8x2^{11}$	$8x2^{12}$	$8x2^{13}$	$8x2^{14}$	$8x2^{15}$	$8x2^{16}$
1000 (÷9)	OFF*	$9x2^{10}$	$9x2^{11}$	$9x2^{12}$	$9x2^{13}$	$9x2^{14}$	$9x2^{15}$	$9x2^{16}$
1001 (÷10)	OFF*	$10x2^{10}$	$10x2^{11}$	$10x2^{12}$	$10x2^{13}$	$10x2^{14}$	$10x2^{15}$	$10x2^{16}$

Table 3-2 RTI Frequency Divide Rates

RTR[3:0]	RTR[6:4] =							
1010 (÷11)	OFF*	$11x2^{10}$	$11x2^{11}$	$11x2^{12}$	$11x2^{13}$	$11x2^{14}$	$11x2^{15}$	$11x2^{16}$
1011 (÷12)	OFF*	$12x2^{10}$	$12x2^{11}$	$12x2^{12}$	$12x2^{13}$	$12x2^{14}$	$12x2^{15}$	$12x2^{16}$
1100 (÷ 13)	OFF*	$13x2^{10}$	$13x2^{11}$	$13x2^{12}$	$13x2^{13}$	$13x2^{14}$	$13x2^{15}$	$13x2^{16}$
1101 (÷14)	OFF*	$14x2^{10}$	$14x2^{11}$	$14x2^{12}$	$14x2^{13}$	$14x2^{14}$	$14x2^{15}$	$14x2^{16}$
1110 (÷15)	OFF*	$15x2^{10}$	$15x2^{11}$	$15x2^{12}$	$15x2^{13}$	$15x2^{14}$	$15x2^{15}$	$15x2^{16}$
1111 (÷ 16)	OFF*	$16x2^{10}$	$16x2^{11}$	$16x2^{12}$	$16x2^{13}$	$16x2^{14}$	$16x2^{15}$	$16x2^{16}$

* Denotes the default value out of reset.This value should be used to disable the RTI to ensure future backwards compatibility.

3.3.9 CRG COP Control Register (COPCTL)

This register controls the COP (Computer Operating Properly) watchdog.

Address Offset: $_08

	7	6	5	4	3	2	1	0
R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-9 CRG COP Control Register (COPCTL)

Read: anytime

Write: once in user mode, anytime in special mode

WCOP — Window COP Mode Bit

When set, a write to the ARMCOP register must occur in the last 25% of the selected period. A write during the first 75% of the selected period will reset the part. As long as all writes occur during this window, $55 can be written as often as desired. Once $AA is written after the $55, the time-out logic restarts and the user must wait until the next window before writing to ARMCOP. **Table 3-3** shows the exact duration of this window for the seven available COP rates.

1 = Window COP operation
0 = Normal COP operation

RSBCK — COP and RTI stop in Active BDM mode Bit

1 = Stops the COP and RTI counters whenever the part is in Active BDM mode.
0 = Allows the COP and RTI to keep running in Active BDM mode.

CR[2:0] — COP Watchdog Timer Rate select

These bits select the COP time-out rate (see **Table 3-3**). The COP time-out period is OSCCLK period divided by CR[2:0] value. Writing a nonzero value to CR[2:0] enables the COP counter and starts the time-out period. A COP counter time-out causes a system reset. This can be avoided by periodically (before time-out) reinitializing the COP counter via the ARMCOP register.

Table 3-3 COP Watchdog Rates[1]

CR2	CR1	CR0	OSCCLK cycles to time-out
0	0	0	COP disabled
0	0	1	2^{14}
0	1	0	2^{16}
0	1	1	2^{18}
1	0	0	2^{20}
1	0	1	2^{22}
1	1	0	2^{23}
1	1	1	2^{24}

NOTES:
1. OSCCLK cycles are referenced from the previous COP time-out reset (writing $55/$AA to the ARMCOP register)

3.3.10 Reserved Register (FORBYP)

NOTE: *This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special modes can alter the CRG's functionality.*

Address Offset: $_09

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-10 Reserved Register (FORBYP)

Read: always read $00 except in special modes

Write: only in special modes

3.3.11 Reserved Register (CTCTL)

NOTE: *This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special test modes can alter the CRG's functionality.*

Address Offset: $_0A

	7	6	5	4	3	2	1	0
R	1	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-11 Reserved Register (CTCTL)

Read: always read $80 except in special modes

Write: only in special modes

3.3.12 CRG COP Timer Arm/Reset Register (ARMCOP)

This register is used to restart the COP time-out period.

Address Offset: $_0B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-12 ARMCOP Register Diagram

Read: always reads $00

Write: anytime

When the COP is disabled (CR[2:0] = "000") writing to this register has no effect.

When the COP is enabled by setting CR[2:0] nonzero, the following applies:

Writing any value other than $55 or $AA causes a COP reset. To restart the COP time-out period you